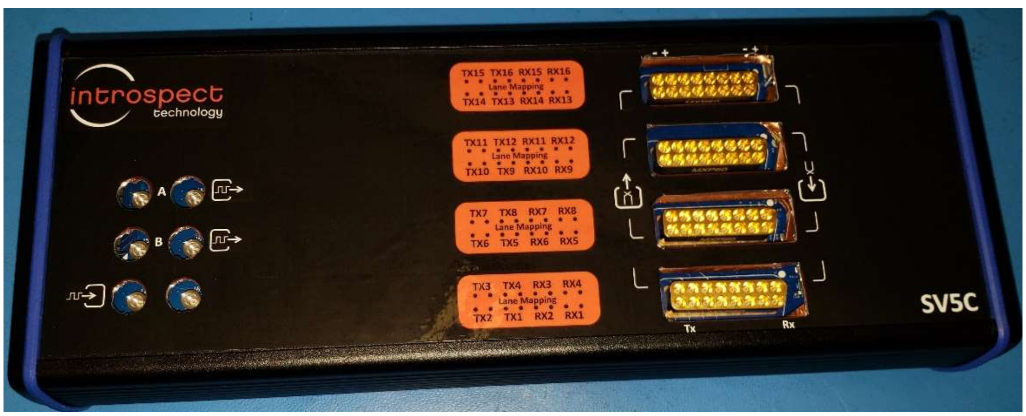
SV5C Personalized SerDes Tester



Data Sheet

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Introduction

Overview

The SV5C is a massively parallel tester that meets the emerging test and validation requirements of increasingly complex electronic component and board designs. Operating at up to 17 Gbps and featuring 16 independent pattern generators and 16 independent signal/data analyzers, the SV5C is the only parallel, phase-aligned BERT in the industry, providing self-contained test and measurement capabilities for testing SerDes interfaces such as PCIe Gen 4, MIPI M-PHY, and USB3. The SV5C also includes unique technologies that allow it to tackle advanced protocols such as DDR4 and DDR5. The SV5 integrates multiple tools into one, providing unprecedented insight into crosstalk and channel-to-channel variations in highly parallel systems.

Key Benefits

- Highest performance SerDes test solution available in a handheld form factor.
- Pattern generators offer voltage, timing, and noise injection controls in ful parallel operation.
- TX amplitude, common-mode voltage and skew control provided on a per-lane basis
- Fully-synthesized integrated jitter injection on all lanes
- Flexible pre-emphasis, equalization, and clock recovery per lane
- TX and RX phase alignment across all channels
- State of the art programming environment based on the highly intuitive Python language
- Single-ended or differential low-speed digital I/O for test control
- Reconfigurable, protocol customization (on request)

Applications

Parallel PHY validation of SerDes bus standards such as:

- PCI Express (PCIe)
- MIPI M-PHY
- CPRI
- USB
- HDMI
- XAUI
- JESD204B
- DDR4 / DDR5

Interface test of electrical/optical media such as:

- Backplane
- Cable
- CFP MSA, SFP MSA, SFP+ MSA

Plug-and-play system-level validation such as:

- PCI Express (PCIe) Gen1, Gen2, Gen3, Gen4
- USB 3.0, 3.0a, 3.0b
- SATA 3.0
- DDR4/DDR5

Timing verification:

- PLL transfer function measurement
- Clock recovery bandwidth verification
- Frequency ppm offset characterization

Mixed-technology applications:

- High-speed ADC and DAC (JESD204) data capture and/or synthesis
- FPGA-based system development
- Channel and device emulation
- Clock-recovery triggering for external oscilloscope or BERT equipment

Physical Connections

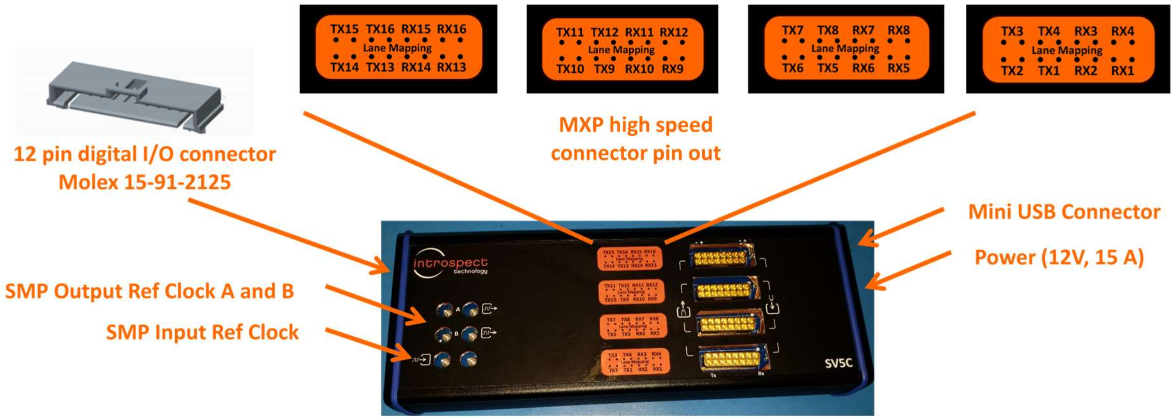


Figure 1 SV5C Physical Connectors

MXP High Speed Connector Pinout

Table 1 Signal mapping of the MXP Connectors for SV5

	MXP 1 Pin	MXP 1 Signal	MXP 2 Pin	MXP 2 Signal	MXP 3 Pin	MXP 3 Signal	MXP 4 Pin	MXP 4 Signal
	1	RX4P	1	RX8P	1	RX12P	1	RX16P
	2	RX4N	2	RX8N	2	RX12N	2	RX16N
MXP	3	RX3P	3	RX7P	3	RX11P	3	RX15P
Top View	4	RX3N	4	RX7N	4	RX11N	4	RX15N
	5	TX4P	5	TX8P	5	TX12P	5	TX16P
	6	TX4N	6	TX8N	6	TX12N	6	TX16N
1 16	7	TX3P	7	TX7P	7	TX11P	7	TX15P
2 15	8	TX3N	8	TX7N	8	TX11N	8	TX15N
3 14	9	TX2N	9	TX6N	9	TX10N	9	TX14N
4 13	10	TX2P	10	TX6P	10	TX10P	10	TX14P
5 12	11	TX1N	11	TX5N	11	TX9N	11	TX13N
6 11	12	TX1P	12	TX5P	12	TX9P	12	TX13P
7 10	13	RX2N	13	RX6N	13	RX10N	13	RX14N
8 9	14	RX2P	14	RX6P	14	RX10P	14	RX14P
	15	RX1N	15	RX5N	15	RX9N	15	RX13N
	16	RX1P	16	RX5P	16	RX9	16	RX13P

Ordering Information

Table 2 Ordering part numbers for the SV5C.

Part Number	Name	Key Differentiators
5712	**SV5C-12 SerDes Tester**	Per channel skew and jitter injection control, 12.5 Gbps maximum data rate
5717	**SV5C-17 SerDes Tester**	Two-bank skew and jitter injection control, 17 Gbps maximum data rate
----	**SV5C Upgrade**	Upgrade option, 12.5 Gbps to 17 Gbps as above

Ordering Information:

XSoptix

800 Village Walk #316
Guilford, CT 06437
Ph: 203-401-8093

Email orders to: sales@xsoptix.com
Fax orders to: 800-878-7282

Features

Transmitter and Receiver

The SV5C includes enhanced transmitter features which allow for maximum flexibility when interfacing to various types of devices under test. A simplified block diagram is shown in Figure 2 below. Each of the features described below may be controlled on a per-channel basis.

The driver may be programmed with a differential amplitude ranging from 0 to 500 mV (single ended) or 1000 mVpp (differential). The driver includes an internal FIR filter, providing two pre-taps and two-post taps for driver pre-emphasis and de-emphasis of the TX signal. The TX common mode voltage offset of the driver may be set from 0 mV to 850 mV.

In addition, an AC noise generator may be used to inject sinusoidal jitter onto the transmitted signal. The frequency of this AC noise is equal to the data rate divided by 16 (i.e., 1 GHz at 16 Gbps operation). This noise may be injected as common mode noise (identical polarity on P and N) or differential noise (opposite polarity on P and N). The maximum amplitude of this noise is 20 mV pp as common mode noise, or 40 mV pp as differential noise.

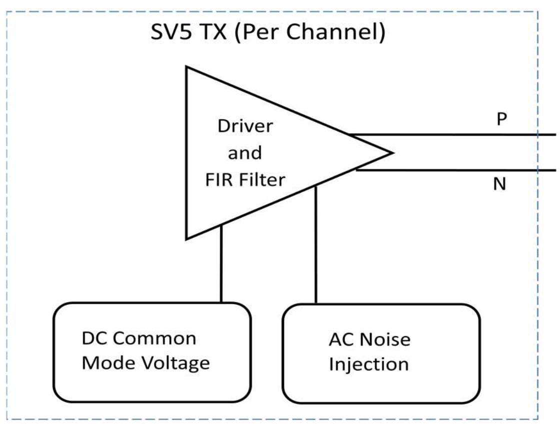
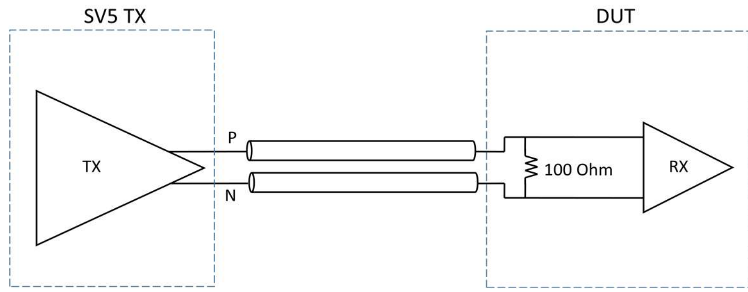
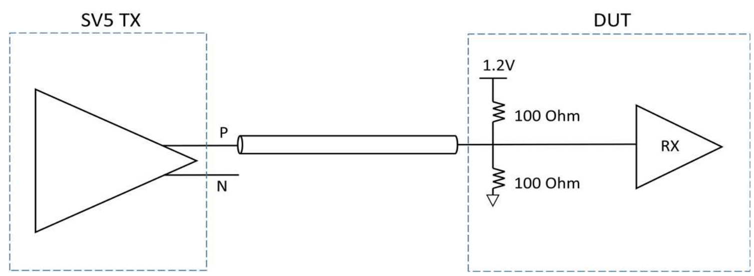


Figure 2 Simplified Block Diagram for SV5C TX.

Figure 3 shows examples of typical device interconnection for both differential and single ended test cases. For differential cases, such as CML or LVDS signalling, direct connection between the SV5 and DUT may be made. For single ended signalling (such as DDR, as shown) the negative signal from the SV5 may be left floating. Other DDR type terminations, such as Series-Stub Termination (SSTL) may also be used with the SV5.



(a)



(b)

Figure 3 Typical connection to the SV5 TX: (a) Differential LVDS and (b) Signal Ended DDR.

Figure 4 shows examples of typical device interconnection to the SV5 receiver, for both differential and single ended cases. For differential cases, such as CML or LVDS signalling, direct connection between the SV5 and DUT may be made. For single ended signalling (such as DDR) the negative signal from the SV5 may be left floating, but it is recommended that the negative signal be AC coupled to ground, if possible, for optimal signal integrity.

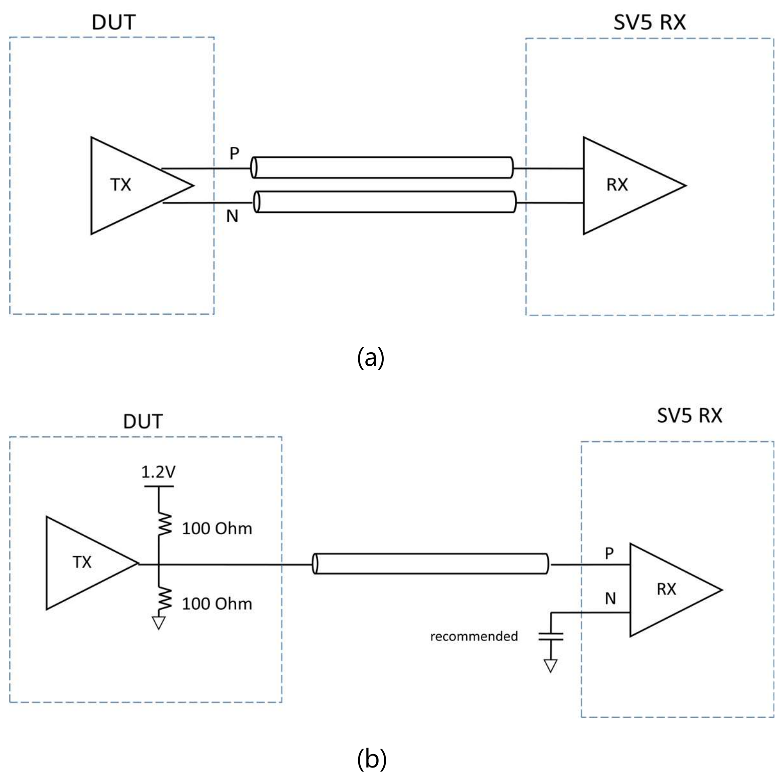


Figure 4 Typical connection to the SV5 RX: (a) Differential LVDS or CML and (b) Signal Ended DDR.

Standard Error Detector Analysis

The SV5C instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Shmoos of various kinds

Figure 5 illustrates a few of the analysis and reporting features of the SV5C. Starting from the top left and moving in a clock-wise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, eye diagram plotting and raw data viewing. As always, these analysis options are executed in parallel on all activated lanes.

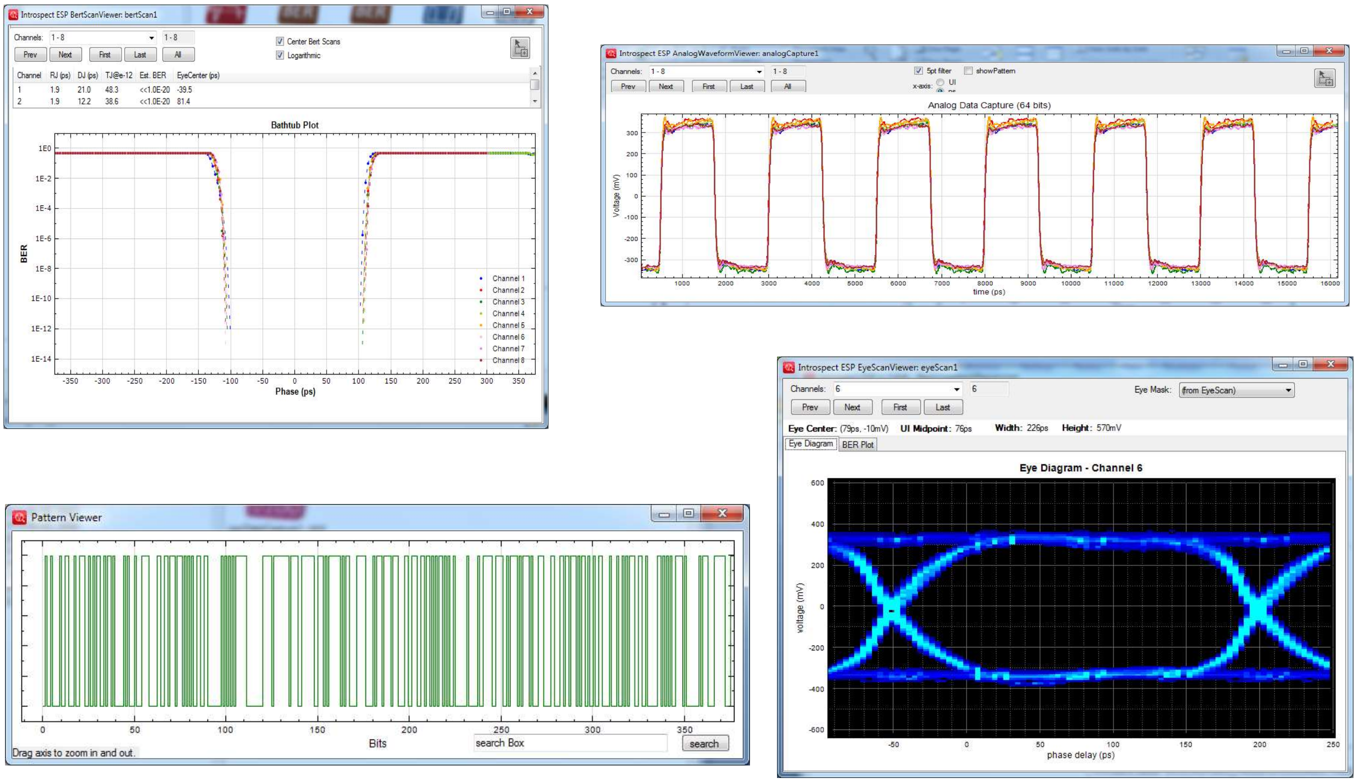


Figure 5 Sampling of analysis and report windows.

Per-Lane Clock Recovery and Unique Dual-Path Architecture

True to the integrated nature of its design, each SV5C receiver has its own embedded analog clock recovery circuit. That is, 16 individual CDR circuits are monolithically integrated in this miniature test system, thus offering the lowest possible sampling latency in a test and measurement instrument.

The monolithic nature of the SV5C clock recovery helps achieve wide tracking bandwidth for measuring signals that possess spread-spectrum clocking or very high amplitude wander. Figure 6 shows a block diagram of the clock recovery capability inside the SV5C Personalized SerDes Tester. Also shown in Figure 6 is the dual-path receiver architecture of the SV5C. This unique architecture allows the SV5C to operate as both a digital capture/analysis instrument and an analog measurement instrument. A feature rich clock management system allows for customization of the SV5C to specific customer requirements.

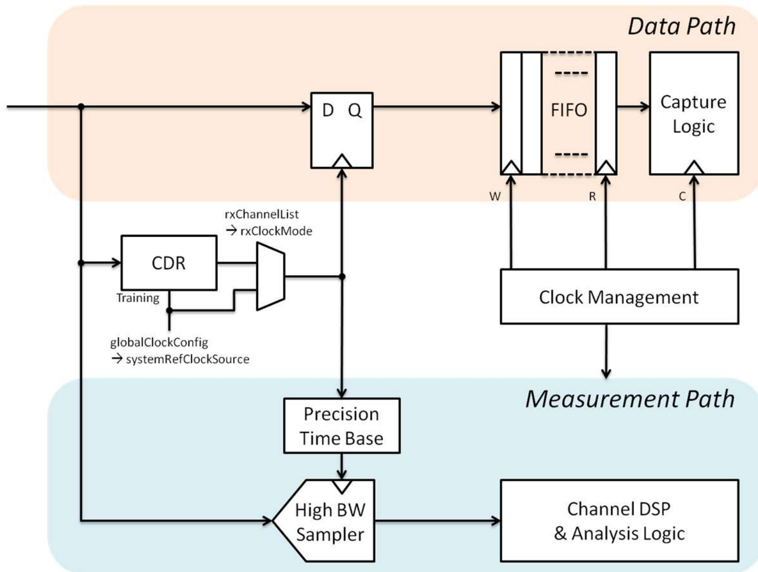


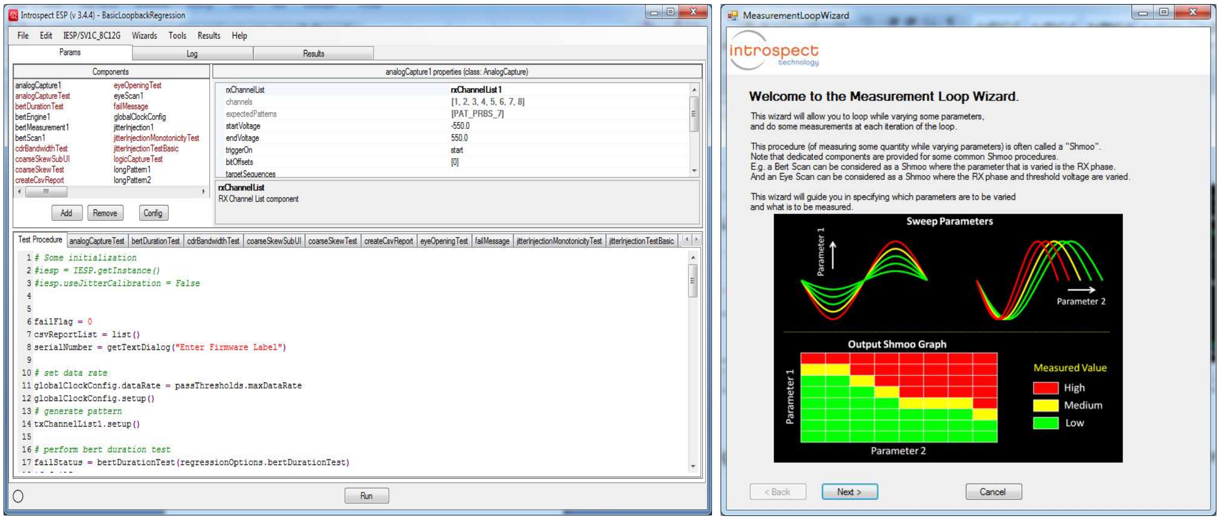
Figure 6 Per-lane clock recovery and dual-path architecture.

Digital I/O Pins

In order to support test automation and a self-contained bench environment, the SV5C Personalized SerDes Tester includes reconfigurable digital I/O pins for simple device controls. Such processing can include generating simple triggers and flags, controlling device resets and relay matrices. The available I/O pins are customizable on request and can configured to support input, output, single-ended, or differential configurations. A miniature12-pin cable connector is provided for rapid prototyping on low-speed signals (as shown previously in Figure 1). The part number for the SV5 miniature 12-pin cable connector is Molex 15-91-2125. Contact the factory for digital I/O customization.

Automation

The SV5Cis operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot inFigure 7(a). Component-based design is Introspect ESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV5C features wizard-based code generation for highly automated tasks such as measurement loops(illustrated in Figure 7(b)).



(a) *(b)*

Figure 7 Screen captures of Introspect ESP user environment.

Specifications

Table 3 General Specifications

Parameter		Value	Units	Description and Conditions
Ports				
	Number of Differential Transmitters	16		
	Number of Differential Receivers	16		
	Number of Dedicated Clock Outputs	2		Individually synthesized frequency and output format.
	Number of Dedicated Clock Inputs	1		Used as external Reference Clock input.
	Number of Trigger Input Pins	Multiple		Contact factory for customization.
	Number of Flag Output Pins	Multiple		Contact factory for customization.
Power	Voltage Supply	12 V		
	Current Draw	5.7 A		5 Gbps / 16 channel TX and RX operation, typical
		6.6 A		12.5 Gbps / 16 channel TX and RX operation, typical
Data Rates and Frequencies				
	Minimum Programmable Data Rate	400	Mbps	Contact factory for extension to lower data rates.
	Maximum Programmable Data Rate	17	Gbps	
	Maximum Data Rate Purchase Options	12.5	Gbps	
		17	Gbps	
	Data Rate Field Upgrade			Upgrade available for 12.5-17 Gbps. Contact factory for details.
	Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
	Minimum External Input Clock Frequency	25	MHz	
	Maximum External Input Clock Frequency	250	MHz	
	Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
	Minimum Output Clock Frequency	10	MHz	
	Maximum Output Clock Frequency	500	MHz	
	Output Clock Frequency Resolution	1	kHz	
	Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and LVCMOS.

Table 4 Transmitter Characteristics

Parameter		Value	Units	Description and Conditions
Output Coupling				
	AC Output Differential Impedance	100	Ohm	Typical
HS Output Coupling				
	Output Single-Ended Impedance	50	Ohm	Typical
	Output Impedance Tolerance	+/- 5	Ohm	
HS Voltage Performance	Minimum Single-Ended Voltage Swing	0	mV	Specifies the available swing on top of any common mode level
	Maximum Single-Ended Voltage Swing	500	mV	Specifies the available swing on top of any common mode level
	Voltage Resolution	10	mV	
	Accuracy of Voltage Programming	larger of: +/- 10 % and +/- 10mV	%, mV	
	Minimum Common Mode Voltage	0	mV	
	Maximum Common Mode Voltage	850	mV	
	Common Mode Voltage Resolution	1	mV	
	Common Mode Voltage Accuracy	larger of: +/- 20 % and +/- 20mV	%, ps	
	Rise and Fall Time	60	ps	
	Swing and Common Mode Level Setting	Per lane		
HS Pre-emphasis Performance				
	Pre-Emphasis Pre-Tap1 Range	TBD	dB	Target pre-emphasis range of Post-Tap 1 for TX amplitude of 800 mV is 3 dB. All pre-emphasis subject to characterization.
	Pre-Emphasis Pre-Tap1 Resolution	TBD	dB	
	Pre-Emphasis Pre-Tap2 Range	TBD	dB	
	Pre-Emphasis Pre-Tap2 Resolution	TBD	dB	
	Pre-Emphasis Post-Tap1 Range	TBD	dB	
	Pre-Emphasis Post-Tap1 Resolution	TBD	dB	
	Pre-Emphasis Post-Tap2 Range	TBD	dB	
	Pre-Emphasis Post-Tap2 Resolution	TBD		
	Pre-Emphasis Level Setting	Per lane		
HS Jitter and Noise Performance				
	Random Jitter Noise Floor	0.8	ps	Based on a single-lane measurement with high-bandwidth scope and with first-order clock recovery.
	Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	
	Maximum Frequency of Injected Deterministic Jitter	50	MHz	
	Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	
	Maximum Peak-to-Peak Injected Deterministic Jitter	1000 500	ps ps	
	Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection frequencies less than 1 MHz. Jitter injection frequencies less than 10 MHz.
	Accuracy of Injected Jitter Magnitude	larger of: +/-10% and +/- 10ps	%, ps	

Max Amplitude of Injected Noise			
Common Mode	20	mV	
Differential	40	mV	
Amplitude Resolution of Injected Noise:	1	mV	
Frequency of Injected Noise	data rate / 16	GHz	
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Coarse (Integer-UI) Min Programmable Skew Range	-20 to 20	UI	
Lane to Lane Coarse (Integer-UI) Resolution	1	UI	
Lane to Lane Fine Skew Min Programmable Skew Range	-500 to 500	ps	
Lane to Lane Fine Skew Resolution	1	ps	
Effect of Skew Adjustment on Jitter Injection	None		

Table 5 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
AC Input Differential Impedance	100	Ohm	
AC Performance			
RX Threshold Range	-400 to 400	mVdiff	
RX Threshold Resolution	20 mV		
Accuracy of Threshold Voltage Programming	larger of: +/- 15 % and +/- 15 mV	%, ps	
Minimum Detectable Differential Voltage	90	mV	
Maximum Allowable Differential Voltage	1200	mV	
Resolution Enhancement & Equalization			
DC Gain	0, 3, 6, 8, 10	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Jitter Performance			
Input Jitter Noise Floor in System Reference Mode	2	ps	Based on a single-lane measurement.
Input Jitter Noise Floor in Extracted Clock Mode	1	ps	Based on a single-lane measurement.
Timing Generator Performance			
Resolution at Maximum Data Rate	7.8125	mUI	Resolution (as a percentage of UI) improves for lower data rates. Contact factory for details.
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		

Table 6 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	1		All sites operate at same frequency.
Frequency Resolution of Programmed Data Rate	1	kbps	

Revision Number	History	Date
1.0	Document release.	September 4, 2018
1.1	Updates to overview and specifications.	September 11, 2018

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