introspect technology

DATA SHEET

SV4E-SLVSEC

16-Lane, 6.5 Gbps SLVS-EC Protocol Analyzer

E SERIES

Published in Canada on August 9, 2021
EN-D054E-E-21236

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Introduction

OVERVIEW

The **SV4E-SLVSEC 16-Lane, 6.5 Gbps Protocol Analyzer** is a highly integrated packet and protocol analyzer that enables the development, debugging, and testing of image sensor and camera systems based on the Scalable Low Voltage Signaling Embedded Clock (SLVS-EC) Version 2.0 protocol. This protocol is also referred to as the JIIA EVI-001-2019, and it was published recently by the Japan Industrial Imaging Association. The SV4E-SLVSEC's unique analog front-end technology provides high-confidence design validation at speeds far exceeding the latest SLVS-EC standards. The Introspect ESP Software provided with the analyzer includes a full suite of tools and viewers for packet analysis, error detection and payload extraction. Key applications include both chip-level level and module-level testing for image sensors and high-end vision systems.

KEY FEATURES

- **Physical Layer Receiver**: up to 16 receiver lanes operating at 6.5 Gbps per lane and featuring integrated per-lane clock recovery
- **Complete Protocol Flexibility:** sophisticated analysis core provides support for basic and multiple-interface topologies that are integrated into the most advanced image sensor architectures
- **Capture Memory**: 8 GBytes of available memory for complete data capture (headers, payloads, and footers) spanning multiple image frames at high resolutions
- **Diagnostics**: Detailed data analysis including payload extraction and error detection
- **I2C Master**: built-in I2C controller for programming sensors and providing true host-emulation capability integrated within the Introspect ESP Software
- **Programmable Power Supplies**: six built-in power supplies for devices under test, with control and current monitoring functions integrated within the Introspect ESP Software

KEY BENEFITS

- **Self-Contained**: an all-in-one system enables the simplest bench environment for protocol validation applications
- **Automated**: leverages the full power of Python and the award-winning Introspect ESP Software. Scripting capability is ideal for debug tasks and full-fledged production screening of devices and system modules
- **Multiple Interface Topologies**: protect your investment by adopting a high-performance tool for multiple applications and across a large span of sensor topologies

ORDERING INFORMATION

TABLE 1 ITEM NUMBERS FOR THE SV4E-SLVSEC ANALYZER

PART NUMBER	NAME	KEY DIFFERENTIATORS
6802	SV4E-SLVSEC Analyzer (includes Introspect ESP SW license)	Full-featured protocol analyzer for SLVS-EC applications
4854	PV2 Universal Active Probe	8 GHz bandwidth, compatible with any oscilloscope and with any Introspect Technology instrument

Ordering Information:

XSoptix

800 Village Walk #316
Guilford, CT 06437
Ph: 203-401-8093

Email orders to: sales@xsoptix.com
Fax orders to: 800-878-7282

Product Feature Description

SLVS-EC RECEIVER IMPLEMENTATION

The SV4E-SLVSEC Protocol Analyzer includes a completely integrated 16 lane receiver containing both an analog front end and digital hardware analysis engine. Each lane of the analog front end features a linear amplifier, a continuous-time linear equalizer, a high performance clock and data recovery (CDR) circuit with phase and voltage threshold comparator controls. A block diagram of the analog front end is shown in the block diagram in Figure 1 below.

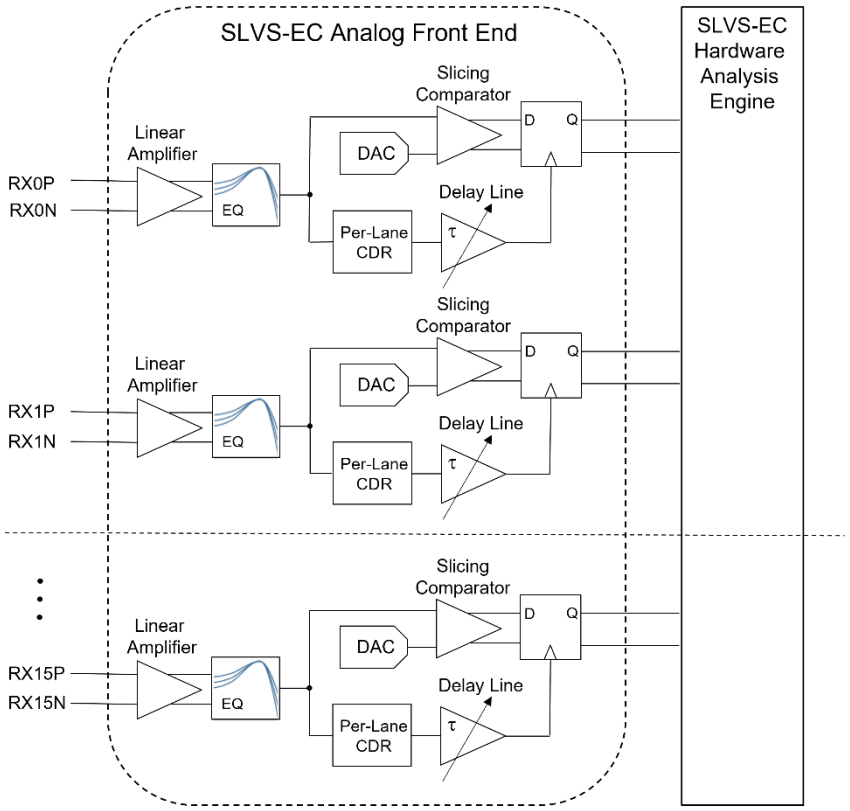
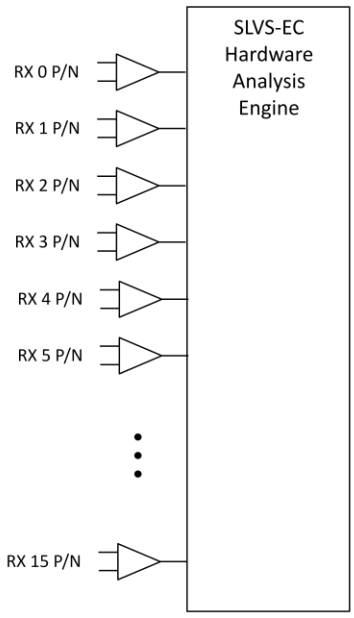


Figure 1: Block diagram of the SV4E-SLVSEC analog front end

SLVS-EC INTERFACE TOPOLOGIES

The SV4E-SLVS-EC Protocol Analyzer supports several interface topologies. Single interface topologies support 2, 4, or 8 lanes, while multiple interface topologies support up to 16 lanes. The assignment of lanes in each case is shown in Figure 2 below. For detailed pinout locations, please refer to the "SV4E-SLVSEC Analyzer Reference Design Guide" as listed under "Additional Documentation" on page 14 of this document.



Single Interface Topology

Lane Names	Lane Count Assignment		
	2	4	8
RX 0 P/N	x	x	x
RX 1 P/N	x	x	x
RX 2 P/N		x	x
RX 3 P/N		x	x
RX 4 P/N			x
RX 5 P/N			x
RX 6 P/N			x
RX 7 P/N			x

Multiple Interface Topology

Lane Names	Lane Count Assignment				
	2	4	8	12	16
RX 0 P/N	x	x	x	x	x
RX 1 P/N		x	x	x	x
RX 2 P/N			x	x	x
RX 3 P/N			x	x	x
RX 4 P/N				x	x
RX 5 P/N				x	x
RX 6 P/N					x
RX 7 P/N					x

Lane Names	Lane Count Assignment				
	2	4	8	12	16
RX 8 P/N	x	x	x	x	x
RX 9 P/N		x	x	x	x
RX 10 P/N			x	x	x
RX 11 P/N			x	x	x
RX 12 P/N				x	x
RX 13 P/N				x	x
RX 14 P/N					x
RX 15 P/N					x

Figure 2: SV4E-SLVSEC lane assignment for both single-interface and multiple interface topologies

DATA CAPTURE AND ANALYSIS TOOLS

The SV4E-SLVSEC Analyzer integrates a hardware analysis engine that makes it a complete physical layer, link layer, and protocol analysis solution. An overview of the analysis features available for data captures is shown in Figure 3, which includes viewers for:

- Packets: byte and symbol level traffic for each lane may be viewed and searched, active payloads are extracted and errors (payload CRC) are automatically highlighted
- Bursts: the bit-level raw incoming data stream may be viewed and searched per lane
- Frames: images are automatically reconstructed and saved, even if incomplete, and details such as pixel formats and image dimensions are displayed

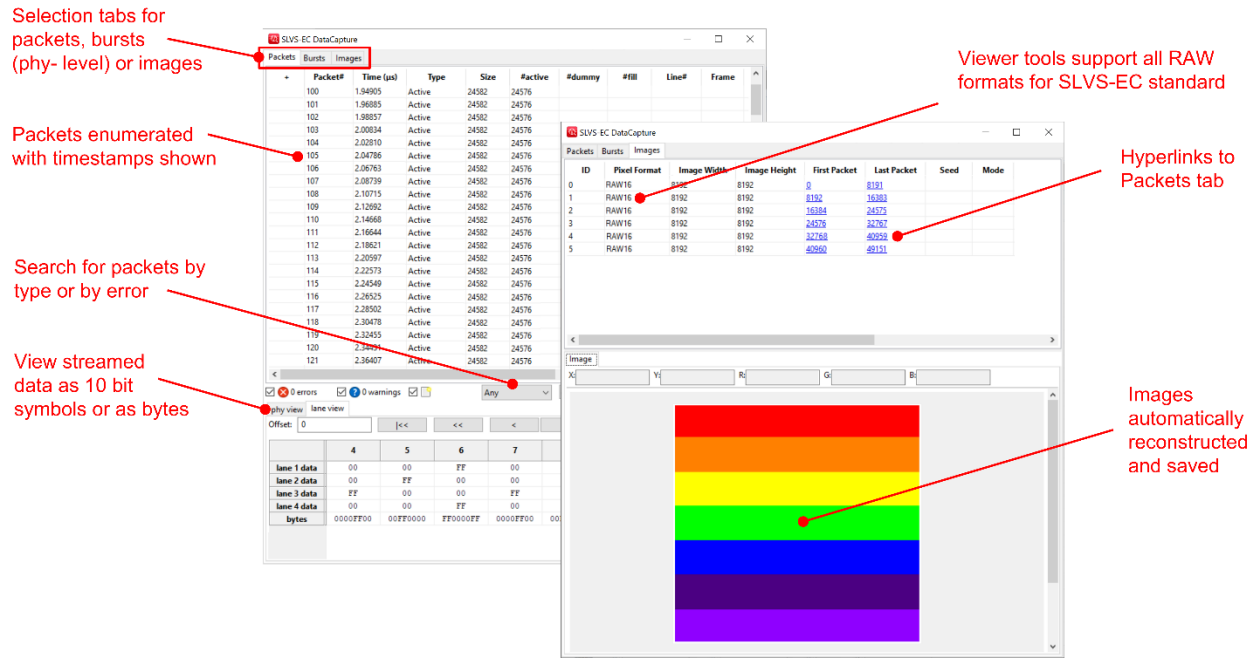


Figure 3: Packet and frame viewers in the Introspect ESP Software

ADVANCED TRIGGER MODES FOR DATA CAPTURE

Data captures may be set up in a few quick steps in the Introspect ESP software as shown in Figure 4 below. A data capture test procedure may be as simple as two lines of Python code as shown at the bottom left of the figure. Trigger conditions are chosen by selecting the "data capture" component at the top left of the figure. Trigger conditions may be modified in the component properties as shown on the top right and will apply whenever the "captureMode" is set to "burst" as in the figure.

Table 2 provides a list of trigger conditions that are available in the Analyzer. Triggering may be based on events (for example, a frame start), on symbols (startCode or other specified dataSymbol) or on errors (crcError or headerCrcError). The duration of data captured **preceding** the trigger event (in ns) is specified by the "preTriggerDuration" setting.

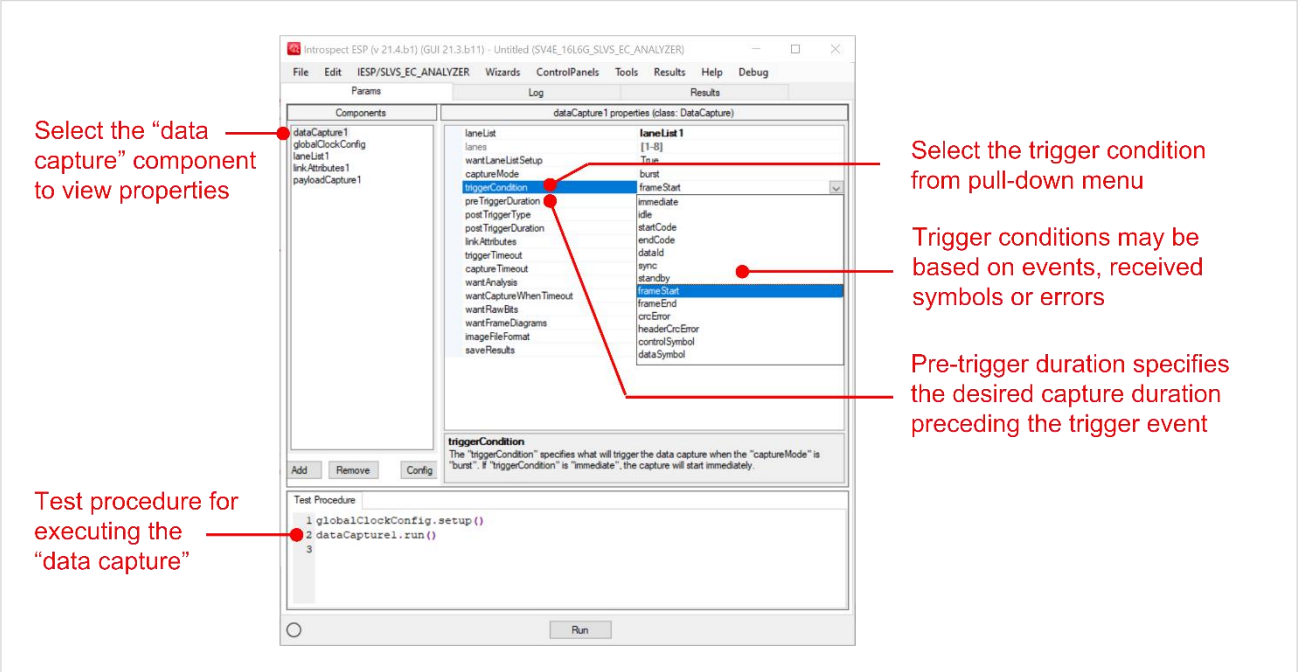


Figure 4: Introspect ESP Software GUI for the SV4E-SLVSEC, showing the trigger options for a data capture

TABLE 2: TRIGGER CONDITIONS

TRIGGER CONDITION NAME	TYPE OF EVENT	TRIGGER DESCRIPTION
immediate	Time-Based	Time-based acquisition, beginning immediately
idle	PHY Control Code	Detection of idle code other than in a packet transfer (four 8b10b symbols)*
startCode	PHY Control Code	Detection of the start control code at start of packet transfer (four 8b10b symbols)*
endCode	PHY Control Code	Detection of the end control code at end of packet transfer (four 8b10b symbols)*
sync	PHY Control Code	Detection of sync control code (four 8b10b symbols)*
standBy	PHY Control Code	Detection of standby control code (four 8b10b symbols)*
controlSymbol	PHY Control Code	Detection of a user-specified control symbol (one 8b10b symbol)
frameStart	Header Information	Detection of a Frame Start bit in packet header
frameEnd	Header Information	Detection of a Frame End bit in packet header
dataId	Header Information	Detection of user-defined integer value in a packet header (specified as an integer)
dataSymbol	Packet Data	Detection of user-defined valid packet data symbol (specified as an integer)
headerCrcError	Error	Detection of CRC error in a packet header
crcError	Error	Detection of CRC error in packet payload

* Control codes as defined by SLVS-EC Standard Version 2.0

SPECIFYING THE ACQUISITION DURATION FOR A DATA CAPTURE

The duration of a data capture **following** the trigger event is determined according to the "postTriggerType", as shown in Figure 5 on the following page. Table 3 provides the full list of conditions for determining the acquisition duration.

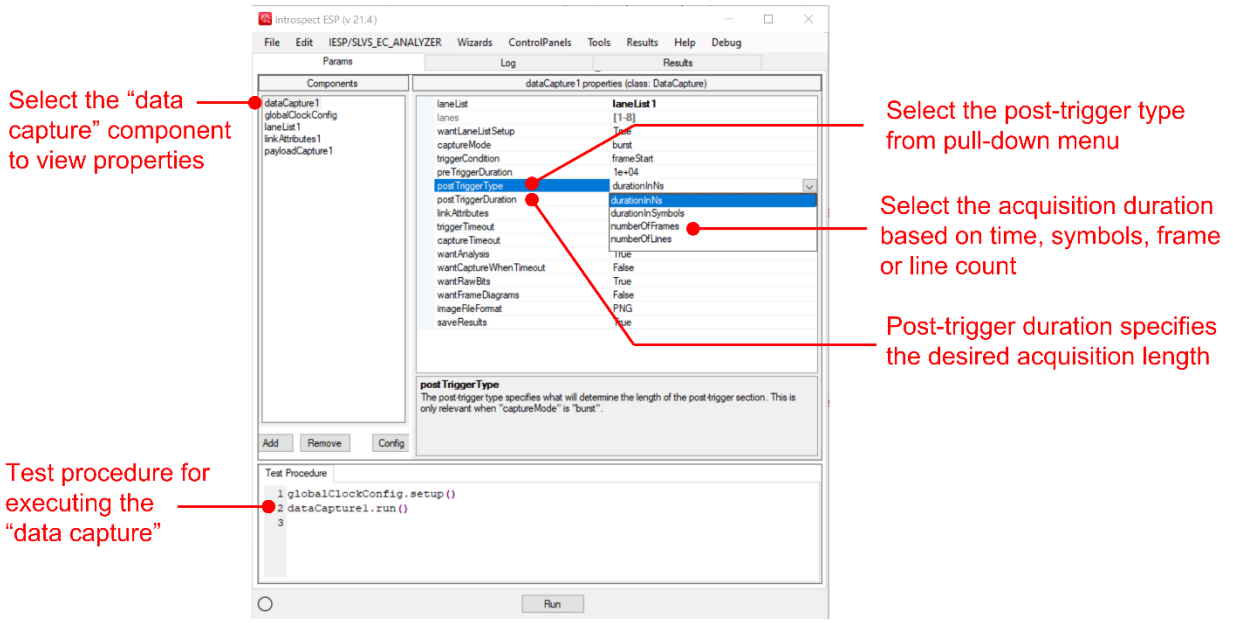


Figure 5: Introspect ESP Software GUI for the SV4E-SLVSEC, showing the post-trigger options for a data capture

TABLE 3: SPECIFICATION OF ACQUISITION DURATION

SPECIFICATION OF ACQUISITION DURATION	ACQUISITION DURATION DESCRIPTION
durationInNs	Post-trigger acquisition length defined in nanoseconds
durationInSymbols	Post-trigger acquisition length defined by the total number of symbols received across all data lanes
numberOfLines	Post-trigger acquisition length defined by the total number of received packets (lines)
numberOfFrames	Post-trigger acquisition length defined by the total number of received frames

PAYLOAD CAPTURE FOR IMAGE DATA

The payload capture feature may be used to capture a set of contiguous image frames without detailed packet analysis results. Payload captures may be set up in a few quick steps in Introspect ESP software as shown in Figure 6 below. The output of a payload capture is a standard image file.

A payload capture test procedure may be as simple as two lines of Python code as shown at the bottom left of the figure below. The payload capture is always triggered by the first valid "frame start" detected in the received data, and the acquisition duration is specified by the "capture timeout" as shown on the top right of the figure. Several output file formats are available from the "imageFileFormat" pull-down menu. Output files are written into a single time-stamped entry in the "Results" output file folder associated with the test procedure.

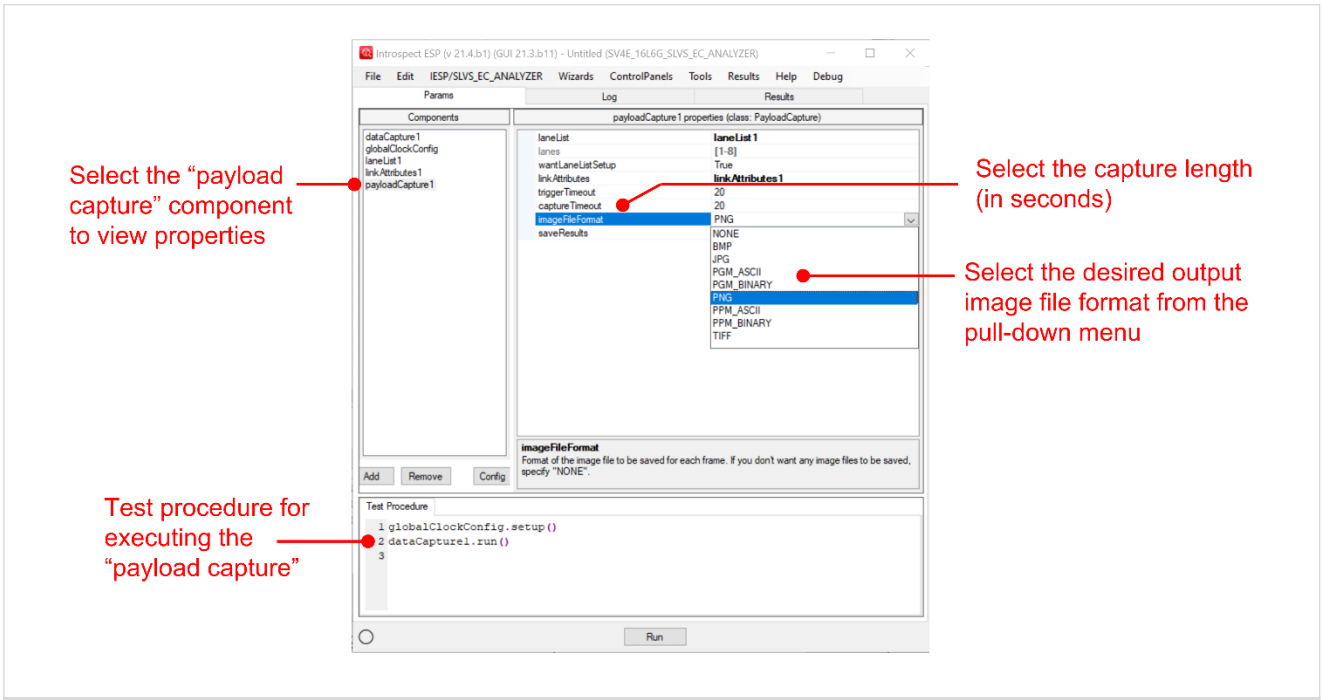


Figure 6: Introspect ESP Software GUI for the SV4E-SLVSEC, showing the setup for a payload capture

Ports and Connectors

For benchtop applications, the SV4E-SLVSEC is enclosed in external casing as shown in Figure 7. All of the SV4E ports and connectors are accessible on the left and right sides of the module, as shown in the figure.

For ATE applications where the external casing of the SV4E may not be required, ports may be directly accessed at the circuit board level. Please refer to the "SV4E-SLVSEC Reference Design Guide" as listed under "Additional Documentation" on the following page of this document.

Figure 7: SV4E-SLVSEC ports and connectors: (a) USB and power (b) High and low speed connectors

HIGH SPEED CONNECTORS

The SV4E-SLVSEC has two 26 pin high speed connectors for SLVS-EC inputs. These connectors provide 16 lanes of SLVS-EC data at a maximum bandwidth of 6.5 Gbps. Please refer to the "SV4E-SLVSEC Reference Design Guide" for physical connector and pinout information, as well as to Figure 2 on page 6 of this document for the high speed receiver implementation.

LOW SPEED CONNECTORS

The SV4E-SLVSEC has one 40 pin low speed connector which provides 16 general purpose I/Os (GPIO) and 6 programmable power supplies.

GPIO pins are provided for communications with DUTs, external devices, or other automated test equipment. The first five GPIOs on the SV4E-SLVSEC are reserved, while the remaining 11 GPIOs are user-defined and may operate as either input or output. All pins operate at 2.5 V CMOS voltage levels.

TABLE 4: SV4E GPIO ADDITIONAL PIN DESCRIPTIONS

GPIO PIN NAME	STATUS	I/O	DESCRIPTION
RESET_N	Reserved	I	SV4E reset pin, active low (“0” = reset, “1” = not in reset)
USER I2C SCL	Reserved	O	General purpose I2C bus (SV4E is master)
USER I2C SDA	Reserved	I/O	General purpose I2C bus (SV4E is master)
FRAME_START/END	Reserved	O	Asserted to “1” on frame start, deasserted to “0” on frame end
LINE_START/END	Reserved	O	Asserted to “1” on line start, deasserted to “0” on line end
GPIO[5] to GPIO[15]	User Configurable	I/O	Input or output

Six programmable power supplies are provided for powering a DUT or for powering other external devices. The programmable range of these supplies is from 1.0V to 5.0V, in steps of 1 mV, with a maximum output current of 3.0 A for each supply. Both voltage programming and current monitoring are provided through the Introspect ESP Software interface, and each supply may be programmed independently.

Please refer to the “SV4E-SLVSEC Reference Design Guide” as listed below for full information on physical connector and pinout information.

Additional Documentation

SV4E-SLVSEC Reference Design Guide

- EN-G054E-E-21235 - SV4E-SLVSEC Reference Design Guide

Reference document for physical dimensions, ports, and connector pinouts. The document provides information for both benchtop and ATE applications.

Specifications

TABLE 5: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Physical Layer Interface	SLVS-EC		Version 2.0
Ports			
Number of Receiver Lanes	16		High Speed Differential Pairs
Number of GPIO pins	16		Low Speed Single Ended
Pre-Defined GPIO pins	5		SV4E RESET (input) I2C Bus (SCL, SDA, master only) FRAME_START (output) LINE_START (output)
User-Defined GPIO	11		Configurable, input or output, for use as triggers or flags
Programmable On-Board Power Supplies	6		
Connections to PC for Introspect ESP Software Control	2		USB2 and USB3
Data Transfer Rate via USB3	350	MBytes/sec	Typical transfer rate for image data from SV4E-SLVSEC to user PC over USB3 connection
Power Consumption			
DC Input Voltage	12	V	
Maximum Current Draw	TBD	A	
Symbol Rates / Frame Rates			
Minimum Data Rate	1.2	Gbps	Per Lane
Maximum Data Rate	6.5	Gbps	Per Lane

TABLE 6: HIGH SPEED RECEIVER SPECIFICATION

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Impedance	50	ohm	
High Speed Input Voltage			
Minimum $\|V_{ID}\|$	100	mV	Measured at SV4E module connector
Maximum $\|V_{ID}\|$	1000	mV	Measured at SV4E module connector
Skew Tolerance			
Maximum Inter-pair Skew	10	UI	Independent internal CDR per lane

TABLE 7: GENERAL PURPOSE I/O SPECIFICATION

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	2.5	V	All GPIOs operate at 2.5 V LVCMOS
V_{IL} minimum	-0.3	V	
V_{IL} maximum	0.7	V	
V_{IH} minimum	1.7	V	
V_{IH} maximum	3.3	V	
V_{OL} maximum	0.4	V	
V_{OH} minimum	2.0	V	

TABLE 8: PACKET AND FRAME ANALYSIS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Features			
Supported Pixel Formats	RAW, RGB*		RAW8, RAW10, RAW12, RAW14, RAW16 RGB888*
Packet Analysis	Yes		Header and payload extraction Dummy and fill detection
Frame Analysis	Yes		Image width / height detection Pixel format detection
CRC Analysis	Yes		Header and payload error detection Packet error statistics
Data Capture Trigger Conditions			Refer to Table 2
Data Capture Acquisition Duration			Refer to Table 3
Output Image File Format			BMP, JPEG, PGM, PNG, PPM, TIFF
Memory Depth	8	GBytes	For received packet data

* not part of the SVLS-EC standard

TABLE 9: PROGRAMMABLE POWER SUPPLY SPECIFICATION

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Performance			
Number of Power Supplies	6		Each supply programmed independently
Minimum Voltage	1000	mV	
Maximum Voltage	5000	mV	
Voltage Programming Resolution	1	mV	
Maximum Output Current	3.0	A	Per supply
Current Measurement Capability	Yes		Independent measurement provided on each programmable supply
Minimum Current Measurement	50	mA	
Current Measurement Resolution	4	mA	

Revision Number	History	Date
1.0	Document Release	August 9, 2021

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Published in Canada on August 9, 2021
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