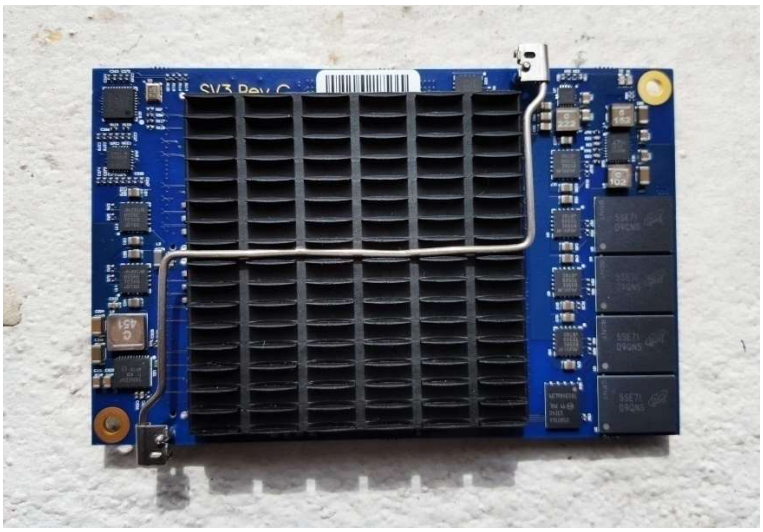
SV3D Direct-Attach SerDes Module



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Introduction

Overview

The SV3DDirect-Attach SerDes Module is a versatile, high-performance instrument that creates a new category of tool for high-speed digital product engineering teams. It integrates multiple technologies to enable the self-contained test and measurement of SerDes interfaces such as PCI Express Gen 3, MIPI M-PHY or USB3 and advanced protocols such as MIPI C-PHY and MIPI D-PHY. The SV3Dmounts directly on an application or test board without cables. It contains 32 independent SerDes stimulus generation ports, 32 independent capture and measurement SerDes ports and various clocking, synchronization and lane-expansion capabilities. It has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection and jitter measurement.

With a small footprint, an extensive signal-integrity feature set, and an exceptionally powerful software development environment, the SV3D is not only suitable for signal-integrity verification engineers that perform traditional characterization tasks, but it is also ideal for FPGA developers and software developers who need rapid turnaround signal verification tools or hardware-software interoperability confirmation tools. The SV3D integrates state of the art functions such as digital data capture, bit error rate measurement, clock recovery, jitter decomposition and jitter generation.

Key Benefits

- True parallel bit-error-rate measurement across 32 lanes
- Fully-synthesized integrated jitter injection on all lanes
- Fully-automated integrated jitter testing on all lanes
- Optimized pattern generator rise-time for receiver stress test applications
- Flexible pre-emphasis and equalization
- Flexible loopback support per lane
- Hardware clock recovery per lane
- State of the art programming environment based on the highly intuitive Python language
- Integrated device control through SPI, I2C, or JTAG
- Reconfigurable, protocol customization (on request)
- Reconfigurable GPIOs
- RoHS Compliant (meets 2011/65/EU RoHS Directive)

Applications

Parallel PHY validation of serial bus standards such as:

- PCI Express (PCIe)
- UHS-2
- MIPI M-PHY
- CPRI
- USB
- HDMI
- Thunderbolt
- XAUI
- JESD204B
- SATA

Interface test of electrical/optical media such as:

- Backplane
- Cable
- CFP MSA, SFP MSA, SFP+ MSA

Plug-and-play system-level validation such as:

- PCI Express
- MIPI D-PHY, CSI/DSI Protocols
- MIPI M-PHY, Unipro Protocols

Timing verification:

- PLL transfer function measurement
- Clock recovery bandwidth verification
- Frequency ppm offset characterization

Mixed-technology applications:

- High-speed ADC and DAC (JESD204) data capture and/or synthesis
- FPGA-based system development
- Channel and device emulation

Features

Multi-Lane Loopback

The SV3D is the only bench-top tool that offers instrument-grade loopback capability on all differential lanes. The loopback capability of the SV3D includes:

- Retiming of data for the purpose of decoupling DUT receiver performance from DUT transmitter performance
- Arbitrary jitter or voltage swing control on loopback data

Figure 1shows two common loopback configurations that can be used with the SV3D. In the first configuration, a single DUT's transmitter and receiver channels are connected together through the SV3D. In the second configuration, arbitrary pattern testing can be performed on an end-to-end communications link. The SV3D is used to pass data through from a traffic generator (such as an end-point on a real system board) to the DUT while stressing the DUT receiver with jitter, skew, or voltage swing.

Figure 1 Illustration of loopback applications

Multiple-Source Jitter Injection

The SV3D is capable of generating calibrated jitter stress on any data pattern and any output lane configuration. Sinusoidal jitter injection is calibrated in the time and frequency domain in order to generate high-purity stimulus signals as shown inFigure 2.

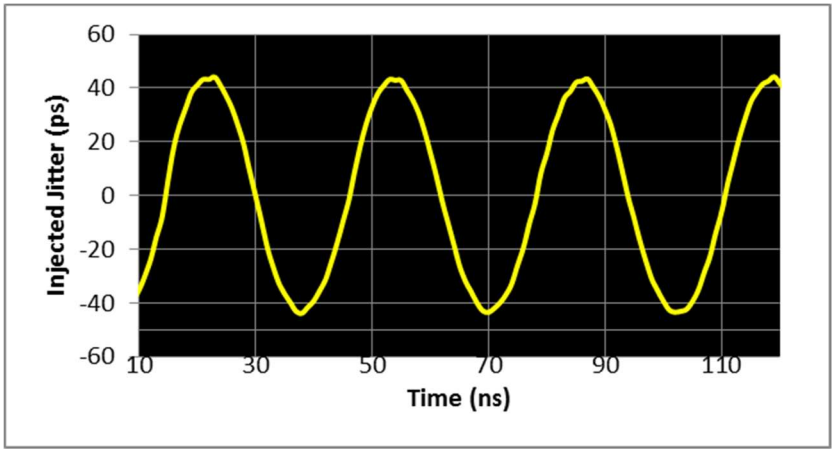


Figure 2 Illustration of calibrated jitter waveform

The jitter injection feature is typically exploited to perform automated jitter tolerance testing as shown in the example inFigure 3. As is the case for other features in the SV3DDirect-Attach SerDes Module, jitter tolerance testing is conducted in parallel across all lanes. For advanced applications, the SV3D also includes RJ injection and a third-source arbitrary waveform jitter synthesizer.

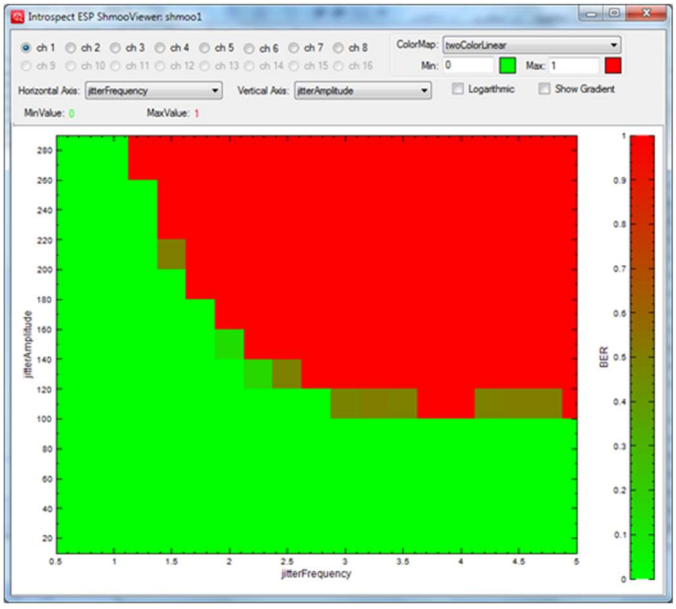


Figure 3 Illustration of jitter tolerance curve

Pre-Emphasis Generation

Conventionally offered as a separate instrument, per-lane pre-emphasis control is integrated on the 8-lane SV3D tester. The user can individually set the transmitter pre-emphasis using a built-in Tap structure. Pre-emphasis allows the user to optimize signal characteristics at the DUT input pins.

Each transmitter in the SV3D implements a discrete-time linear equalizer as part of the driver circuit. An illustration of such equalizer is shown inFigure 4, and sample synthesized waveform shapes are shown inFigure 5.

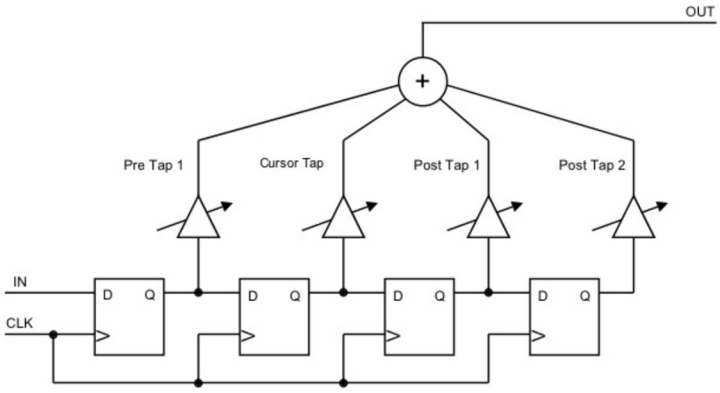


Figure 4 Illustration of pre-emphasis design

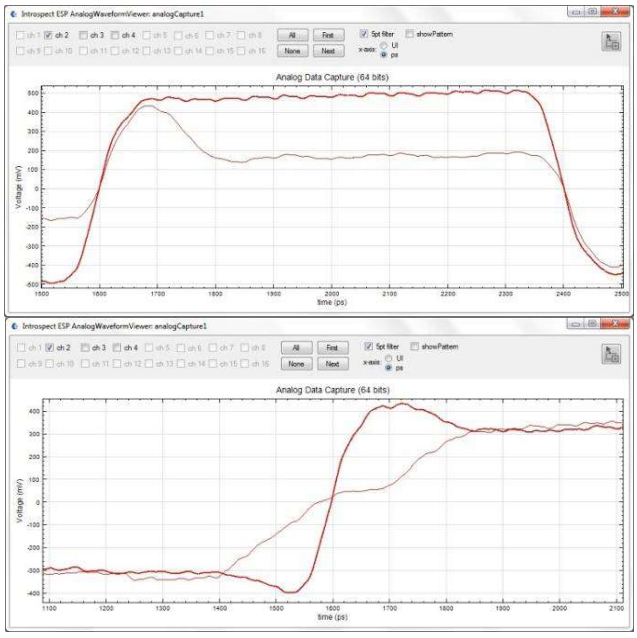


Figure 5 Illustration of multiple waveform shapes that can be synthesized using the pre-emphasis function of the SV3D

Burst-Mode BER Testing

Modern SerDes interfaces require complex training sequences and sophisticated power-efficient operating modes. Often called burst-mode, many SerDes transmissions require a new class of Error Detector: one that is able to compute BER on only sections of a non-continuous transmitted data stream. The SV3D includes the optional ability to automatically track intermittent sleep/burst cycles within a test pattern and to measure only relevant payload sections. This is illustrated in Figure 6. In the figure, the link is asleep for a long time (indicated by the static low and static high levels), then some training "SYNC" pattern is transmitted for a short burst before payload data is transmitted. Once the payload data is transmitted, the SV3C automatically resumes error detection and error counting.

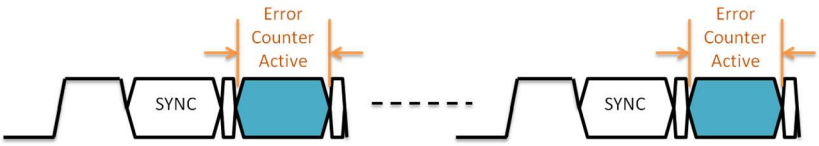


Figure 6 Illustration of burst-mode error detection.

Programmable SSC Generation and Frequency Synthesis

The SV3D incorporates precision frequency synthesis technology that allows for the generation of programmable SSC waveforms at any data rate. The SSC waveforms are superimposed on the pattern generator outputs, and they coexist with other jitter injection sources of the SV3D. Thus, a truly complete jitter cocktail can be produced for the most thorough receiver validation. Figure 7illustrates the SSC capability of the SV3D. In the figure, the SV3D is programmed to synthesize four slightly different modulation frequencies showcasing the precision programmability of the tool.

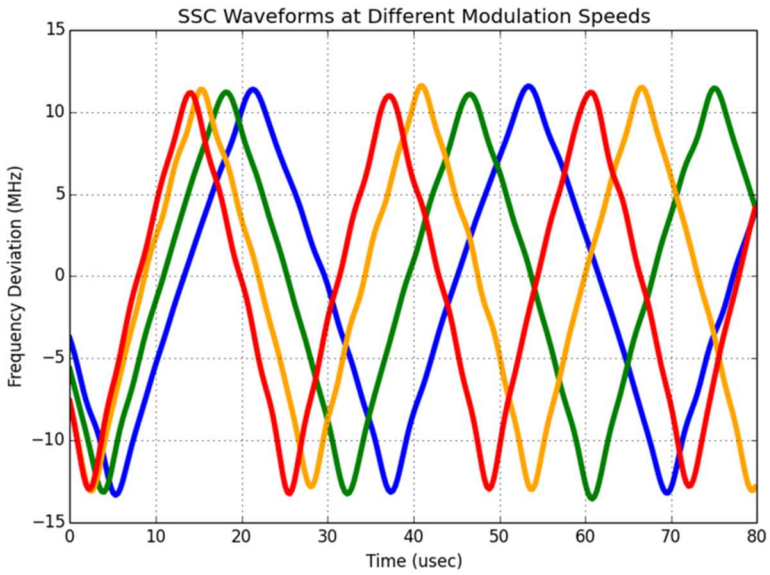


Figure 7 Programmable SSC generation

Per-Lane Clock Recovery and Unique Dual-Path Architecture

True to the integrated nature of its design, each SV3C receiver has its own embedded analog clock recovery circuit. That is, 32 individual CDR circuits are monolithically integrated in this miniature test system, thus offering the lowest possible sampling latency in a test and measurement instrument.

The monolithic nature of the SV3C clock recovery helps achieve wide tracking bandwidth for measuring signals that possess spread-spectrum clocking or very high amplitude wander. Figure 8 shows a block diagram of the clock recovery capability inside the SV3C Personalized SerDes Tester. Also shown in Figure 8 is the dual-path receiver architecture of the SV3C. This unique architecture allows the SV3C to operate as both a digital capture/analysis instrument and an analog measurement instrument. A feature rich clock management system allows for customization of the SV3C to specific customer requirements.

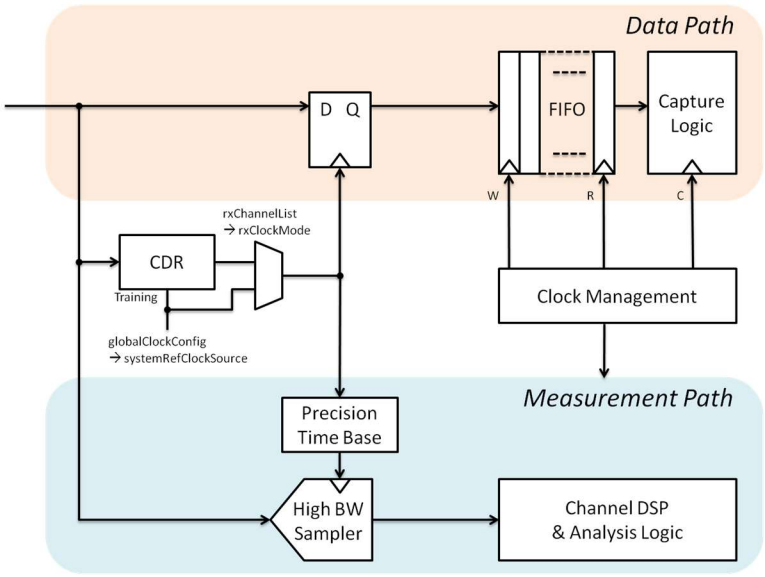


Figure 8 Per-lane clock recovery and dual-path architecture

Auxiliary Control Port

The SV3D includes a low-speed auxiliary control port. It enables controlling DUT registers through JTAG, I2C, or SPI. Additionally, the port includes two reconfigurable trigger and five flag capabilities for synchronizing with external tools or events. The pin location for these controls are as given in Table 6.

Parallel Transfer Interface

The SV3D includes a low-speed, 32 bit wide output parallel interface, for transferring data from the SV3D to a DUT or external device. Data on the 32 bit interface is valid when the PTI_RDEMPTY output pin is low and valid on the rising edge of PTI_CLK input(clock signal provided by the external device). The intended rate of data transfers is 12.5 MHz.Typical transfer waveforms are given inFigure 9 and Figure 10. The pin location for the Parallel Transfer Interface are as given in Table 6.

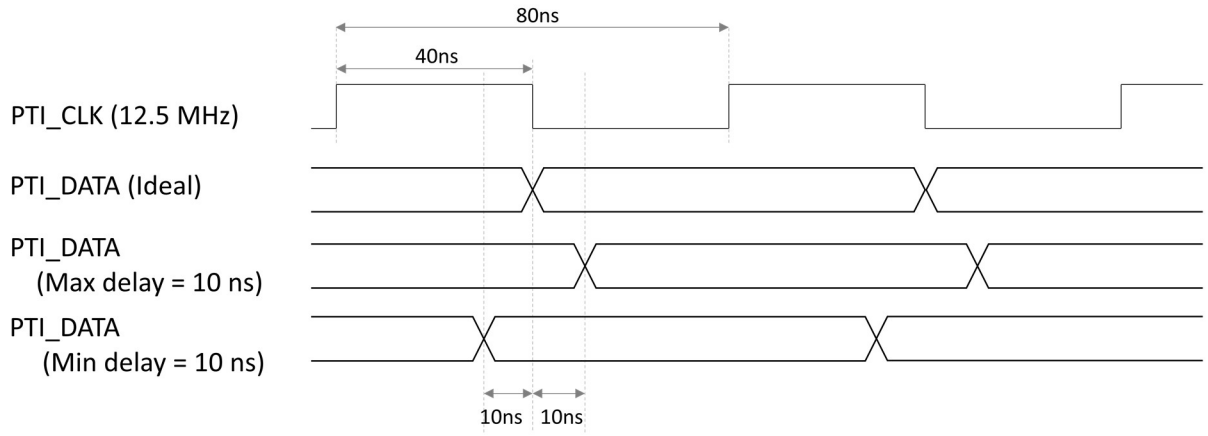
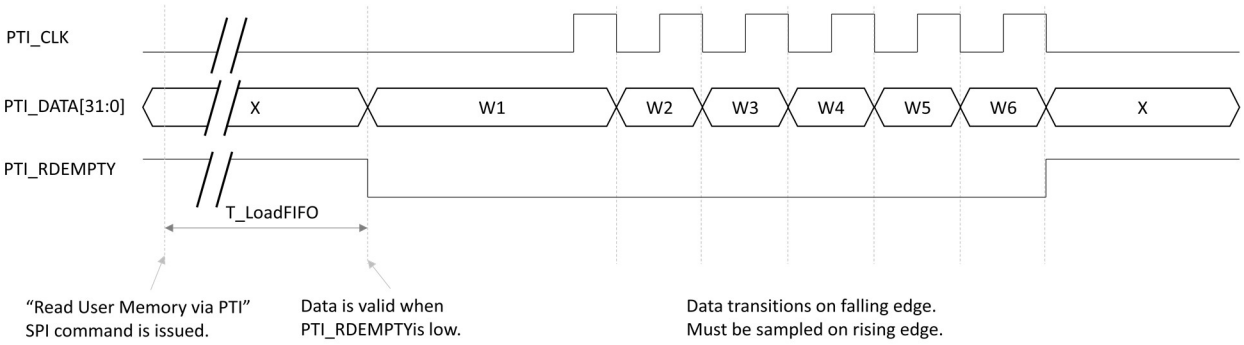


Figure 9 PTI clock / data relationship for 12.5 MHz (single data rate) operation. The same delays apply to PTI_RDEMPTY.



- W1 to W6 are valid 32-bit words. X is invalid data.
- T_LoadFIFO depends on the transfer size.
- PTI_CLKcan start toggling anytime after PTI_RDEMPTYgoes low.

Figure 10 Sample waveform for 24 byte PTI transfer

Standard Error Detector Analysis

The SV3D instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Frequency measurement and SSC profile extraction

Figure 11illustrates a few of the analysis and reporting features of the SV3D. Starting from the top left and moving in a clock-wise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, raw data viewing, and eye diagram plotting. As always, these analysis options are executed in parallel on all activated lanes.

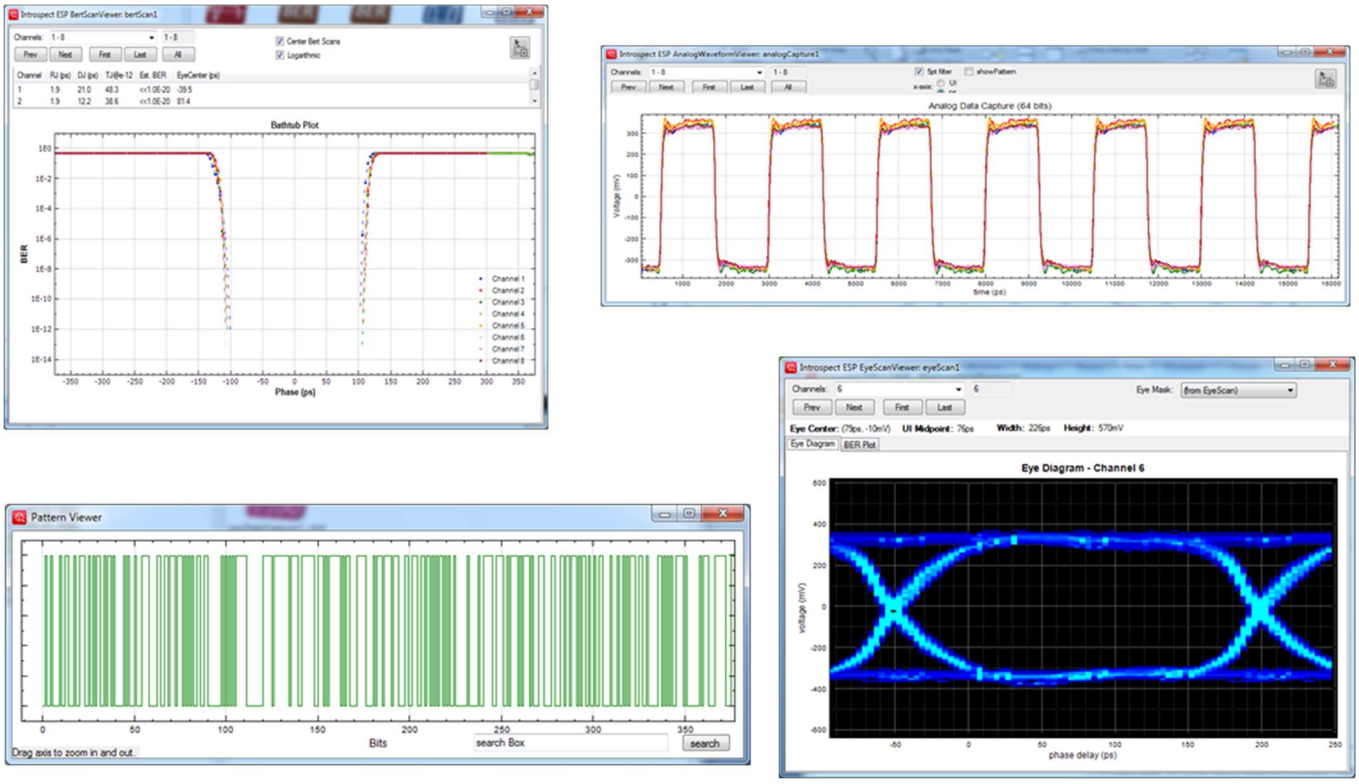
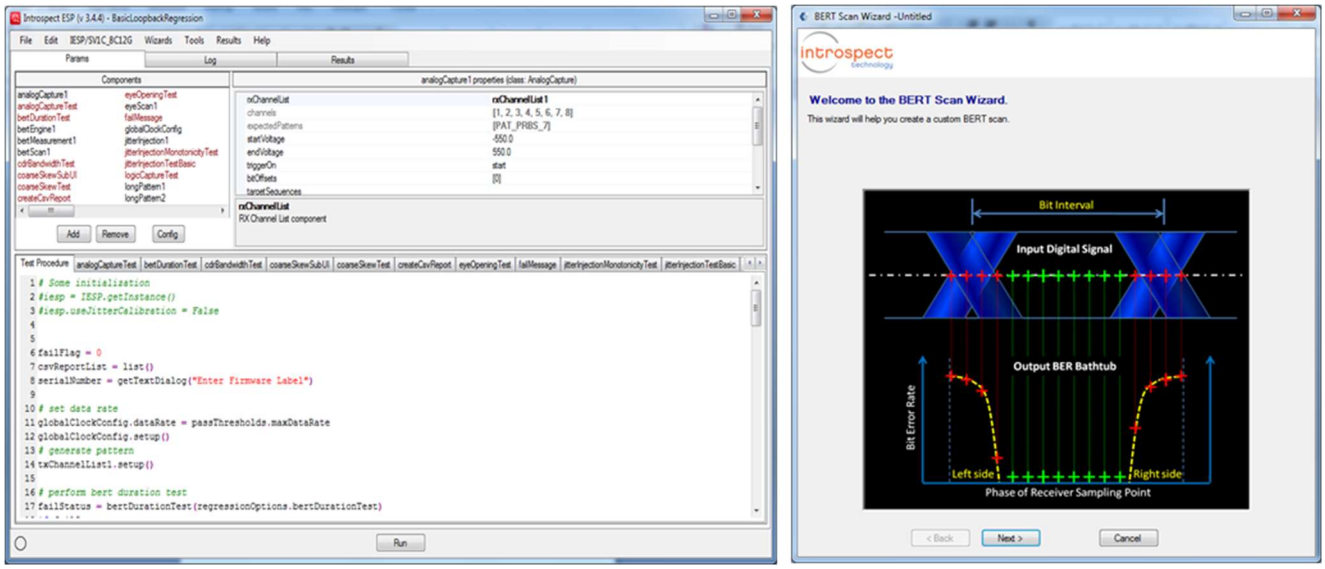


Figure 11 Sampling of analysis and report windows

Automation

The SV3D is operated using the award winning IntrospectESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 12(a). Component-based design is IntrospectESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV3D features automatic code generation for common tasks such as Eye Diagram or Bathtub Curve generation as shown in Figure 12(b).



(a) *(b)*

Figure 12 Screen capture of IntrospectESP user environment.

Physical Description

Figure 13 and Figure 14 depict the top and bottom views of the SV3D module.

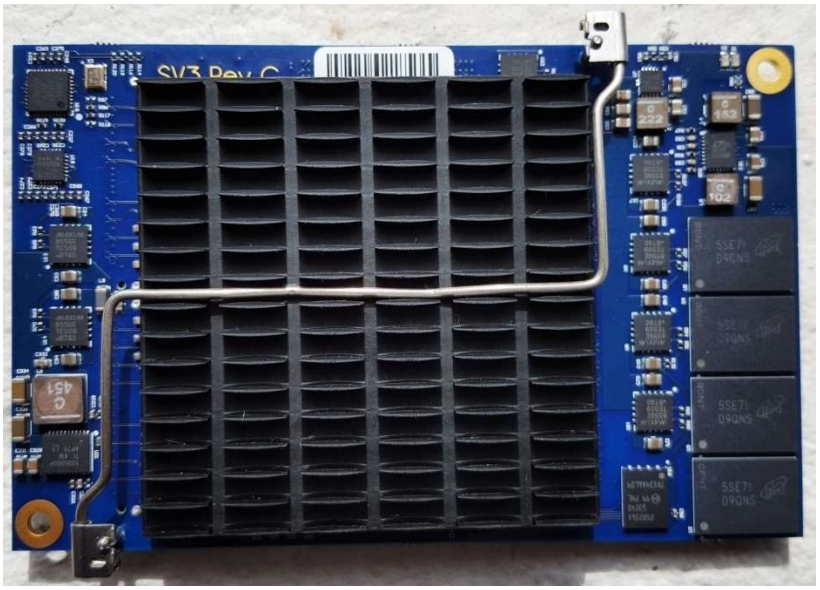


Figure 13 Top view of SV3D module

Figure 14 Bottom view of SV3D module

Loadboard Connectors Footprint and Dimensions

Figure 15 depicts the connectors footprint required to mate with the SV3D module. The rectangle area is occupied by the SV3D module, to be mounted on the loadboard by 2 diagonal mounting holes and 5 connectors J1, J2, J3, J4 and J5.

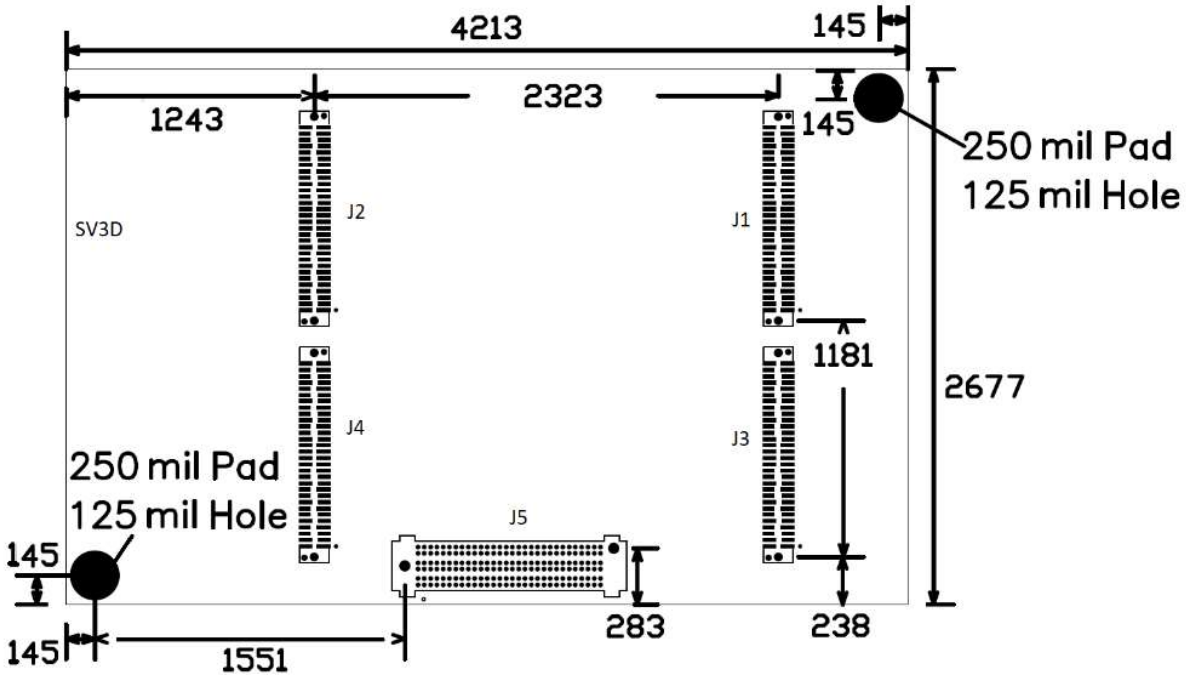


Figure 15 SV3D loadboard footprint placement. Measurements are in mil.

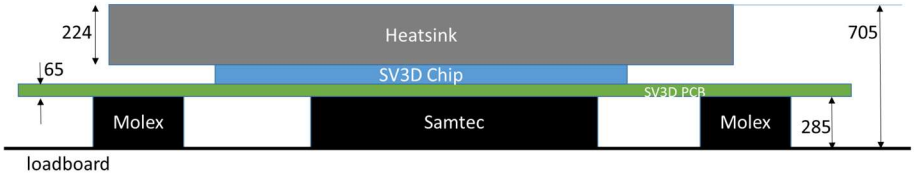


Figure 16 SV3D side profile on loadboard. Measurements are in mil.

The connectors part number information is shown in Table 1.

Table 1 Loadboard Connectors Descriptions

Connector	Manufacturer	Part Number	Descriptions	Pin Count
J1, J2, J3, J4	Molex	171446-0115	SPEEDSTACK PLUG ASSY,30CKT,3MM	60
J5	Samtec	SEAM8-30-02.0-S-06-2-K	CONN SEARAY 30x6, 0.8mm pitch	180

Electrical Description

The following tables describe the pin out information of the 5 connectors on the SV3D depicted in Figure 15. When designing the interface logic, please ensure not to drive any I/O pins on the SV3D until the power rails have been completely powered on.

Table 2 Load board J1 Connector Pin-Out

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	RX17_P	GXB Receive Link	1.5V PCML
3	RX17_N	GXB Receive Link	1.5V PCML
5	RX21_P	GXB Receive Link	1.5V PCML
6	RX21_N	GXB Receive Link	1.5V PCML
8	RX18_P	GXB Receive Link	1.5V PCML
9	RX18_N	GXB Receive Link	1.5V PCML
11	RX19_P	GXB Receive Link	1.5V PCML
12	RX19_N	GXB Receive Link	1.5V PCML
14	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	JTAG-TMS	Built-in Pull-up Resistor10kOhm	2.5V
18	RX20_P	GXB Receive Link	1.5V PCML
19	RX20_N	GXB Receive Link	1.5V PCML
21	RX24_N	GXB Receive Link	1.5V PCML
22	RX24_P	GXB Receive Link	1.5V PCML
24	RX23_N	GXB Receive Link	1.5V PCML
25	RX23_P	GXB Receive Link	1.5V PCML
27	RX22_N	GXB Receive Link	1.5V PCML
28	RX22_P	GXB Receive Link	1.5V PCML
30	JTAG-TCK	Built-in Pull-up Resistor 1kOhm	2.5V
31	JTAG-TDI	Built-in Pull-up Resistor 10kOhm	2.5V
33	TX17_P	GXB Transmit Link	1.5V PCML
34	TX17_N	GXB Transmit Link	1.5V PCML
36	TX21_P	GXB Transmit Link	1.5V PCML
37	TX21_N	GXB Transmit Link	1.5V PCML
39	TX18_N	GXB Transmit Link	1.5V PCML
40	TX18_P	GXB Transmit Link	1.5V PCML
42	TX19_P	GXB Transmit Link	1.5V PCML
43	TX19_N	GXB Transmit Link	1.5V PCML
45	JTAG-TDO	Built-in Pull-up Resistor 21.5kOhm	2.5V
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	TX20_N	GXB Transmit Link	1.5V PCML
50	TX20_P	GXB Transmit Link	1.5V PCML
52	TX24_P	GXB Transmit Link	1.5V PCML
53	TX24_N	GXB Transmit Link	1.5V PCML
55	TX23_N	GXB Transmit Link	1.5V PCML
56	TX23_P	GXB Transmit Link	1.5V PCML
58	TX22_P	GXB Transmit Link	1.5V PCML
59	TX22_N	GXB Transmit Link	1.5V PCML

Table 3 Load board J2 Connector Pin-Out

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	RX25_P	GXB Receive Link	1.5V PCML

3	RX25_N	GXB Receive Link	1.5V PCML
5	RX29_P	GXB Receive Link	1.5V PCML
6	RX29_N	GXB Receive Link	1.5V PCML
8	RX26_P	GXB Receive Link	1.5V PCML
9	RX26_N	GXB Receive Link	1.5V PCML
11	RX30_N	GXB Receive Link	1.5V PCML
12	RX30_P	GXB Receive Link	1.5V PCML
14	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	EXTRA_IO_1	GPIO pin	2.5V LVCMOS
18	RX27_P	GXB Receive Link	1.5V PCML
19	RX27_N	GXB Receive Link	1.5V PCML
21	RX31_P	GXB Receive Link	1.5V PCML
22	RX31_N	GXB Receive Link	1.5V PCML
24	RX28_P	GXB Receive Link	1.5V PCML
25	RX28_N	GXB Receive Link	1.5V PCML
27	RX32_N	GXB Receive Link	1.5V PCML
28	RX32_P	GXB Receive Link	1.5V PCML
30	EXTRA_IO_3	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_0	GPIO pin	2.5V LVCMOS
33	TX25_N	GXB Transmit Link	1.5V PCML
34	TX25_P	GXB Transmit Link	1.5V PCML
36	TX29_P	GXB Transmit Link	1.5V PCML
37	TX29_N	GXB Transmit Link	1.5V PCML
39	TX26_N	GXB Transmit Link	1.5V PCML
40	TX26_P	GXB Transmit Link	1.5V PCML
42	TX30_P	GXB Transmit Link	1.5V PCML
43	TX30_N	GXB Transmit Link	1.5V PCML
45	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	EXTRA_IO_2	GPIO pin	2.5V LVCMOS
49	TX27_N	GXB Transmit Link	1.5V PCML
50	TX27_P	GXB Transmit Link	1.5V PCML
52	TX31_P	GXB Transmit Link	1.5V PCML
53	TX31_N	GXB Transmit Link	1.5V PCML
55	TX28_N	GXB Transmit Link	1.5V PCML
56	TX28_P	GXB Transmit Link	1.5V PCML
58	TX32_P	GXB Transmit Link	1.5V PCML
59	TX32_N	GXB Transmit Link	1.5V PCML

Table 4 Load board J3 Connector Pin-Out

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	TX1_P	GXB Transmit Link	1.5V PCML
3	TX1_N	GXB Transmit Link	1.5V PCML
5	TX2_P	GXB Transmit Link	1.5V PCML
6	TX2_N	GXB Transmit Link	1.5V PCML
8	TX3_N	GXB Transmit Link	1.5V PCML
9	TX3_P	GXB Transmit Link	1.5V PCML
11	TX4_P	GXB Transmit Link	1.5V PCML
12	TX4_N	GXB Transmit Link	1.5V PCML
14	EXTRA_IO_5	GPIO pin	2.5V LVCMOS
15	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
16	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
18	TX8_N	GXB Transmit Link	1.5V PCML
19	TX8_P	GXB Transmit Link	1.5V PCML
21	TX7_N	GXB Transmit Link	1.5V PCML
22	TX7_P	GXB Transmit Link	1.5V PCML
24	TX6_N	GXB Transmit Link	1.5V PCML
25	TX6_P	GXB Transmit Link	1.5V PCML
27	TX5_N	GXB Transmit Link	1.5V PCML
28	TX5_P	GXB Transmit Link	1.5V PCML
30	EXTRA_IO_7	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_4	GPIO pin	2.5V LVCMOS
33	RX1_P	GXB Receive Link	1.5V PCML

34	RX1_N	GXB Receive Link	1.5V PCML
36	RX2_N	GXB Receive Link	1.5V PCML
37	RX2_P	GXB Receive Link	1.5V PCML
39	RX3_P	GXB Receive Link	1.5V PCML
40	RX3_N	GXB Receive Link	1.5V PCML
42	RX4_N	GXB Receive Link	1.5V PCML
43	RX4_P	GXB Receive Link	1.5V PCML
45	EXTRA_IO_6	GPIO pin	2.5V LVCMOS
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	RX8_P	GXB Receive Link	1.5V PCML
50	RX8_N	GXB Receive Link	1.5V PCML
52	RX7_N	GXB Receive Link	1.5V PCML
53	RX7_P	GXB Receive Link	1.5V PCML
55	RX6_P	GXB Receive Link	1.5V PCML
56	RX6_N	GXB Receive Link	1.5V PCML
58	RX5_N	GXB Receive Link	1.5V PCML
59	RX5_P	GXB Receive Link	1.5V PCML

Table 5 Load board J4 Connector Pin-Out

Pin	Net	Description	Voltage Level
1,4,7,10,13,17,20,23,26,29,32, 35,38,41,44,48, 51,54,57,60	GND		
2	TX9_P	GXB Transmit Link	1.5V PCML
3	TX9_N	GXB Transmit Link	1.5V PCML
5	TX10_P	GXB Transmit Link	1.5V PCML
6	TX10_N	GXB Transmit Link	1.5V PCML
8	TX14_N	GXB Transmit Link	1.5V PCML
9	TX14_P	GXB Transmit Link	1.5V PCML
11	TX13_N	GXB Transmit Link	1.5V PCML
12	TX13_P	GXB Transmit Link	1.5V PCML
14	REFIN_CLK_P	Ref Clock Input	3.3V LVDS*
15	REFIN_CLK_N	Ref Clock Input	3.3V LVDS*
16	EXTRA_IO_9	GPIO pin	2.5V LVCMOS
18	TX11_P	GXB Transmit Link	1.5V PCML
19	TX11_N	GXB Transmit Link	1.5V PCML
21	TX15_P	GXB Transmit Link	1.5V PCML
22	TX15_N	GXB Transmit Link	1.5V PCML
24	TX12_P	GXB Transmit Link	1.5V PCML
25	TX12_N	GXB Transmit Link	1.5V PCML
27	TX16_N	GXB Transmit Link	1.5V PCML
28	TX16_P	GXB Transmit Link	1.5V PCML
30	EXTRA_IO_11	GPIO pin	2.5V LVCMOS
31	EXTRA_IO_8	GPIO pin	2.5V LVCMOS
33	RX9_P	GXB Receive Link	1.5V PCML
34	RX9_N	GXB Receive Link	1.5V PCML
36	RX10_N	GXB Receive Link	1.5V PCML
37	RX10_P	GXB Receive Link	1.5V PCML
39	RX14_P	GXB Receive Link	1.5V PCML
40	RX14_N	GXB Receive Link	1.5V PCML
42	RX13_N	GXB Receive Link	1.5V PCML
43	RX13_P	GXB Receive Link	1.5V PCML
45	EXTRA_IO_10	GPIO pin	2.5V LVCMOS
46	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
47	RESERVED	(Not used, install R=0Ω to gnd)	1.5V PCML
49	RX11_N	GXB Receive Link	1.5V PCML
50	RX11_P	GXB Receive Link	1.5V PCML
52	RX15_P	GXB Receive Link	1.5V PCML
53	RX15_N	GXB Receive Link	1.5V PCML
55	RX12_N	GXB Receive Link	1.5V PCML
56	RX12_P	GXB Receive Link	1.5V PCML
58	RX16_P	GXB Receive Link	1.5V PCML
59	RX16_N	GXB Receive Link	1.5V PCML

* *REFIN_CLK_P and REFIN_CLK_N have internal AC coupling.*

Table 6 Load board J5 Connector Pin-Out (All GPIO pins driven at 2.5V LVCMOS)

Pin	Net	Pin	Net	Pin	Net	Pin	Net
1	12V0	61	GPIO_4_3	91	GND	151	GPIO_0_0 / SPI PortA SCLK
2	12V0	62	GPIO_4_4	92	GPIO_3_4	152	GPIO_0_7 / SPI PortA MOSI
3	12V0	63	GPIO_4_11	93	GPIO_3_11	153	GPIO_0_8
4	12V0	64	GPIO_4_12	94	GPIO_3_12	154	GPIO_0_15 / SPI PortB SSN
5	12V0	65	GPIO_4_19	95	GPIO_3_19	155	GND
6	12V0	66	GND	96	GPIO_3_20	156	GPIO_1_20
7	GND	67	GPIO_3_0	97	GPIO_2_0	157	GPIO_0_1 / SPI PortA MISO
8	GND	68	GPIO_3_7	98	GPIO_DQS_2_7	158	GPIO_0_6 / SPI PortA SSN
9	GND	69	GPIO_3_8	99	GPIO_2_8	159	GPIO_DQS_0_9
10	GND	70	GPIO_3_15	100	GPIO_2_15	160	GND
11	GND	71	GND	101	GPIO_2_16	161	GPIO_0_16 / SPI PortB MOSI
12	GND	72	GPIO_4_20	102	GPIO_2_23	162	GPIO_0_23
13	PTI_DATA_0	73	GPIO_3_1	103	GPIO_2_1	163	GPIO_0_2
14	PTI_DATA_1	74	GPIO_3_6	104	GPIO_2_6	164	GPIO_0_5
15	PTI_DATA_2	75	GPIO_3_9	105	GPIO_2_9	165	GND
16	PTI_DATA_3	76	GND	106	GPIO_DQS_2_14	166	GPIO_0_14 / SPI PortB SCLK
17	PTI_DATA_4	77	GPIO_3_16	107	GPIO_2_17	167	GPIO_0_17 / SPI PortB MISO
18	PTI_DATA_5	78	GPIO_3_23	108	GND	168	GPIO_0_22
19	PTI_DATA_6	79	GPIO_3_2	109	GPIO_2_2	169	GPIO_0_3
20	PTI_DATA_7	80	GPIO_DQS_3_5	110	GPIO_2_5	170	GND
21	PTI_DATA_8	81	GND	111	GPIO_2_10	171	GPIO_0_10
22	GPIO_5_14	82	GPIO_3_14	112	GPIO_2_13	172	GPIO_0_13
23	GPIO_5_17	83	GPIO_DQS_3_17	113	GND	173	GPIO_0_18
24	GND	84	GPIO_3_22	114	GPIO_2_22	174	GPIO_0_21
25	PTI_DATA_9	85	GPIO_3_3	**115**	GPIO_2_3 / EXT_TRIG[0]	175	GND
26	PTI_DATA_10	86	GND	**116**	GPIO_2_4 / FLAG[4]	176	GPIO_0_4
27	PTI_DATA_11	87	GPIO_3_10	117	GPIO_2_11	177	GPIO_0_11
28	PTI_DATA_12	88	GPIO_3_13	118	GND	178	GPIO_0_12
29	GND	89	GPIO_3_18	119	GPIO_2_18	179	GPIO_0_19
30	PTI_DATA_13	90	GPIO_3_21	120	GPIO_2_21	180	GPIO_DQS_0_20
31	PTI_DATA_14	61	GPIO_4_3	121	GPIO_1_0 / FLAG[3]	151	GPIO_0_0
32	PTI_DATA_15	62	GPIO_4_4	122	GPIO_1_7	152	GPIO_0_7
33	PTI_DATA_16	63	GPIO_4_11	123	GND	153	GPIO_0_8
34	GND	64	GPIO_4_12	124	GPIO_2_12	154	GPIO_0_15
35	PTI_DATA_17	65	GPIO_4_19	125	GPIO_2_19	155	GND
36	PTI_DATA_18	66	GND	126	GPIO_2_20	156	GPIO_1_20
37	PTI_DATA_19	67	GPIO_3_0	127	GPIO_1_1	157	GPIO_0_1
38	PTI_DATA_20	68	GPIO_3_7	128	GND	158	GPIO_0_6
39	GND	69	GPIO_3_8	129	GPIO_DQS_1_8	159	GPIO_DQS_0_9
40	PTI_DATA_21	70	GPIO_3_15	130	GPIO_1_15	160	GND
41	PTI_DATA_22	71	GND	131	GPIO_1_16	161	GPIO_0_16
42	PTI_DATA_23	72	GPIO_4_20	132	GPIO_1_23	162	GPIO_0_23
43	PTI_DATA_24	73	GPIO_3_1	133	GND	163	GPIO_0_2
44	GND	74	GPIO_3_6	134	GPIO_1_6	164	GPIO_0_5
45	PTI_DATA_25	75	GPIO_3_9	135	GPIO_1_9	165	GND
46	PTI_DATA_26	76	GND	136	GPIO_1_14	166	GPIO_0_14
47	PTI_DATA_27	77	GPIO_3_16	137	GPIO_1_17	167	GPIO_0_17
48	PTI_DATA_28	78	GPIO_3_23	138	GPIO_1_22	168	GPIO_0_22
49	GND	79	GPIO_3_2	139	GPIO_1_2 / EXT_TRIG[1]	169	GPIO_0_3
50	PTI_DATA_29	80	GPIO_DQS_3_5	140	GPIO_1_5 / FLAG[2]	170	GND
51	PTI_DATA_30	81	GND	141	GPIO_1_10	171	GPIO_0_10
52	PTI_DATA_31	82	GPIO_3_14	142	GPIO_DQS_1_13	172	GPIO_0_13
53	PTI_CLK	83	GPIO_DQS_3_17	143	GPIO_1_18	173	GPIO_0_18
54	PTI_RDEMPTY	84	GPIO_3_22	144	GPIO_1_21	174	GPIO_0_21
55	PTI_RESERVED_0	85	GPIO_3_3	145	GPIO_1_3 / FLAG[1]	175	GND
56	PTI_RESERVED_1	86	GND	146	GPIO_1_4 / FLAG[0]	176	GPIO_0_4
57	PTI_RESERVED_2	87	GPIO_3_10	147	GPIO_1_11	177	GPIO_0_11
58	GPIO_4_13	88	GPIO_3_13	148	GPIO_1_12	178	GPIO_0_12
59	GPIO_4_18	89	GPIO_3_18	149	GPIO_1_19	179	GPIO_0_19
60	GPIO_4_21	90	GPIO_3_21	150	GND	180	GPIO_DQS_0_20

Specifications

Table 7 General Specifications

Parameter	Value	Units	Description and Conditions
Ports			
Number of Differential Transmitters	32		See Table 2 to Table 5 for pinout.
Number of Differential Receivers	32		See Table 2 to Table 5 for pinout.
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input. See Table 5 for pinout.
Number of Trigger Input Pins	2		Consult user manual for included capability. See Table 6 for pinout.
Number of Flag Output Pins	5		Consult user manual for included capability. See Table 5 for pinout.
Generic I/O Pins	190		Consult user manual for included capability. See Table 3 to Table 6 for pinout. Contact factory for customization.
Data Rates and Frequencies			
Minimum Programmable Data Rate	250	Mbps	Contact factory for extension to lower data rates.
Maximum Programmable Data Rate	14	Gbps	
Maximum Data Rate Purchase Options	4	Gbps	
	8.5	Gbps	
	12.5	Gbps	
	14	Gbps	
Data Rate Field Upgrade	4-12.5	Gbps	Contact factory for details.
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Minimum External Input Clock Frequency	25	MHz	
Maximum External Input Clock frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Voltage and Current Ratings and Operating Conditions			
Voltage Supply	12	V	See Table 6 for pinout connections.
Current on 12VDC input	2.9	A	Typical power-up condition: -Tx and Rx lanes idle
	3.3	A	Typical operating condition: - All 32 Tx cannels running at 8 Gbps - All 32 Rx channels running BER checking as well as eye diagram measurement at 8 Gbps.
	5.6	A	Maximum operating condition: - All 32 Tx pairs running at 14 Gbps - All 32 Rx pairs running BER checking as well as eye diagram measurement at 8 Gbps.

Table 8 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
Output Standard			
I/O Standard			PCML (Current Mode Logic)
DC common mode voltage	750	mV	Typical (firmware programmable to $V_{OD}/2$)
AC Output Differential Impedance	100	Ohm	Typical
Voltage Performance			
Minimum Differential Voltage Swing	20	mV	
Maximum Differential Voltage Swing	1000 800	mVpp mVpp	312.5 Mbps to 5 Gbps, 50 ohm AC coupled termination. 5 Gbps to 12.5 Gbps, 50 ohm AC coupled termination.
Differential Voltage Swing Resolution	20	mV	
Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/- 10mV	%, mV	
Rise and Fall Time	50	ps	500 mVpp signal, 20-80%, 50 ohm AC coupled termination.
Pre-emphasis Performance			
Pre-Emphasis Pre-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Pre-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post1-Tap Range	0 to 6	dB	Only high-pass function is available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post2-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post2-Tap Resolution	Range / 32	dB	
Jitter Performance			
Random Jitter Noise Floor	1	ps	Based on a single-lane measurement with high-bandwidth scope and with first-order clock recovery.
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	80	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contactfactory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1400	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Per-bank		Common across all channels within a bank.
Maximum RMS Random Jitter Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	

Accuracy of Injected Jitter Magnitude	larger of: +/-10% of programmed value, and +/-10 ps	%, ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	+/- 30	ps	

Table 9 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			This is the impedance between differential wires.
AC Input Differential Impedance	100	Ohm	Receiver inputs are DC-coupled
AC Performance			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Minimum Programmable Comparator Threshold Voltage	-550	mV	
Maximum Programmable Comparator Threshold Voltage	+550	mV	
Differential Comparator Threshold Voltage Resolution	10	mV	
Differential Comparator Threshold Voltage Accuracy	larger of: +/-10% of programmed value, and +/- 10mV	%, mV	
Measured Eye Width Accuracy	10%		Maximum error, 312.5 Mbps – 2.0 Gbps, 200 mVpp minimum input amplitude
	15%		Maximum error, 2.0 Mbps - 5 Gbps, 200 mVpp minimum input amplitude
	25%		Maximum error, 5 Gbps – 12.5 Gbps, 200 mVpp minimum input amplitude
Resolution Enhancement & Equalization			
DC Gain	0, 2, 4, 6, 8	dB	
CTLE Maximum Gain	16	dB	
CTLE Resolution	1	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Jitter Performance			
Input Jitter Noise Floor in System Reference Mode	25	ps	Based on a single-lane measurement.

Input Jitter Noise Floor in Extracted Clock Mode	10	ps	Based on a single-lane measurement.
Timing Generator Performance			
Resolution at Maximum Data Rate	31.25	mUI	Resolution (as a percentage of UI) improves for lower data rates. Contact factory for details.
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		
Skew			
Lane to Lane Skew Measurement Accuracy	+/- 10	ps	

Table 10 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	5		Standard configuration creates one measurement path frequency reference, two output clock frequency references. Contact factory for clock domain customization.
Embedded Clock Applications			
Transmit Timing Modes	System		
	Extracted		Clock can be extracted from one of the data receiver channels in order to drive all transmitter channels.
Receive Timing Modes	System		
	Extracted		All channels have clock recovery for extracted mode operation.
Lane to Lane Tracking Bandwidth	4	MHz	
Single-Lane CDR Tracking Bandwidth	3 - 12	MHz	
Forwarded Clock Applications			
Transmit Timing Modes	System		
	Forwarded		Contact factory for forwarded clock routing recommendations.
Receive Timing Modes	System		
	Forwarded		Contact factory for forwarded clock routing recommendations.
Clock Tracking Bandwidth	4	MHz	Second order critically damped response.
Spread Spectrum Support			
Receive Lanes Track SSC Data	Yes		Requires operation in extracted clock mode.
Transmit Lanes Generate SSC Data	Yes		
Minimum Spread	0.1	%	
Maximum Spread	2	%	
Spread Programming Resolution	0.01	%	
Minimum Spreading Frequency	31.5	kHz	
Maximum Spreading Frequency	63	kHz	

Table 11 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Loopback			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	
Preset Patterns			
Standard Built-In Patterns	All Zeros D21.5 K28.5, K28.7 DIV 16, 20 DIV 40, 50 PRBS 5, 7, 9, 11 PRBS13, 15, 21 PRBS 23, 31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
User-programmable Pattern Memory			
Total Available Memory	4	GBytes	Memory allocation is customizable. Contact factory.
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	512	bits	
Maximum Pattern Segment Size	65536	bits	
Total Memory Space for Transmitters	TBD	Mbits	Memory allocation is customizable. Contact factory.
Total Memory Space for Receivers	TBD	Mbits	Memory allocation is customizable. Contact factory.
Pattern Sequencing			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	4		Typical. Configurable to 1 – 18.This is the number of sequencer slots that can operate at any given time.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
Additional Pattern Characteristics			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	Memory allocation is customizable. Contact factory.

Table 12 Instruction Sequence Cache

Parameter	Value	Units	Description and Conditions
Simple Instruction Cache			
Instruction Learn mode Instruction	Start Stop Replay		
Advanced Instruction Cache			
Local Instruction Storage	1M Instructions		
Instruction Sequence Segments	1000		

Table 13 DUT Control Capabilities

Parameter	Value	Units	Description and Conditions
DUT IEEE-1149-1 (JTAG) Port (Option)			
JTAG-Port Transmit Signals	TCK TRST TDI		
JTAG-Port Receive Signals	TDO		
JTAG-Port Transmit Voltage Swing (Fixed)	0 to 2.5	V	
JTAG-Port Receive Max Voltage Swing	0 to 2.5	V	
TDI Bit Memory	4k		
TDO Bit Memory	4k		
DUT SPI Port (Option)			
SPI Signals	SCLK SSN MISO MOSI		
Voltage Swing (Fixed)	0 to 2.5	V	

Revision Number	History	Date
1.0	Document release	Nov 1, 2016
1.1	Updates to pinout (flags, triggers and PTI) and updates to specifications	Feb 14, 2017
1.2	Consolidated updates	March 10, 2017
1.3	Added reference to RoHS compliance	April 14, 2017

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