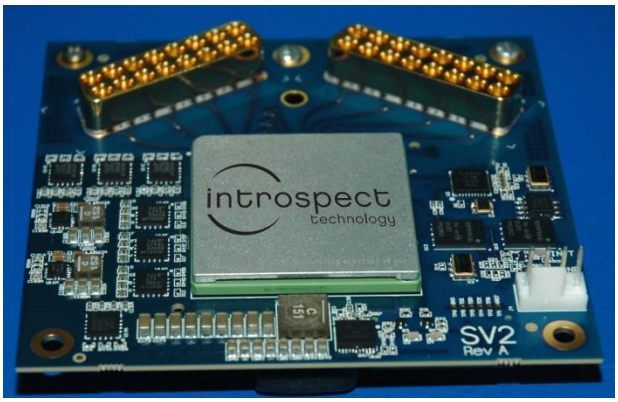
SV2D Direct-Attach SerDes Module



Data Sheet

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Introduction

Overview

The SV2D Direct-Attach SerDes Tester module is a versatile, high-performance instrument for high-speed digital product engineering teams. It integrates multiple technologies to enable the test and measurement of 28 Gbps SerDes interfaces powering next generation telecommunications equipment. Coupled with a seamless, easy-to-use development environment, this tool enables product engineers with widely varying skills to efficiently work with and develop SerDes verification algorithms. The SV2D mounts directly on test applications and contains 8 independent stimulus generation ports, 8 independent error detectors and various clocking, synchronization and lane-expansion capabilities. It has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection, de-emphasis generation, and equalization that closely mimic the final application of the device under test.

With a small footprint, an extensive feature set, and an exceptionally powerful software development environment, the SV2D is not only suitable for receiver signal-integrity verification engineers that perform traditional characterization tasks, but it is also ideal for FPGA developers and software developers who need rapid turnaround signal verification tools or hardware-software interoperability confirmation tools.

Key Benefits

- True parallel bit-error-rate measurement across 8 lanes at up to 28.05 Gbps per lane
- Fully-synthesized integrated jitter injection on all lanes
- Programmable output voltage for receiver stress test applications
- Flexible pre-emphasis and equalization
- Flexible loopback support per lane
- Hardware clock recovery per lane
- State of the art programming environment based on the highly intuitive Python language
- Reconfigurable, protocol customization (on request)

Applications

- Parallel PHY validation of serial bus standards
- Interface tests of electrical/optical media
- At-speed production tests

Features

Simultaneous Parallel Loopback

The SV2D is the only bench-top tool that offers instrument-grade loopback capability on all differential lanes. The loopback capability of the SV2D includes:

- Retiming of data for the purpose of decoupling DUT receiver performance from DUT transmitter performance
- Arbitrary jitter or voltage swing control on loopback data

Figure 1 shows two common loopback configurations that can be used with the SV2D. In the first configuration, a single DUT's transmitter and receiver channels are connected together through the SV2D. In the second configuration, arbitrary pattern testing can be performed on an end-to-end communications link. The SV2D is used to pass data through from a traffic generator (such as an end-point on a real system board) to the DUT while stressing the DUT receiver with jitter, skew, or voltage swing.

Figure 1 Common loopback applications

Multiple-Source Jitter Injection

The SV2D is capable of generating calibrated jitter stress on any data pattern and any output lane configuration. Sinusoidal jitter injection is calibrated in the time and frequency domain in order to generate high-purity stimulus signals as shown in Figure 2.

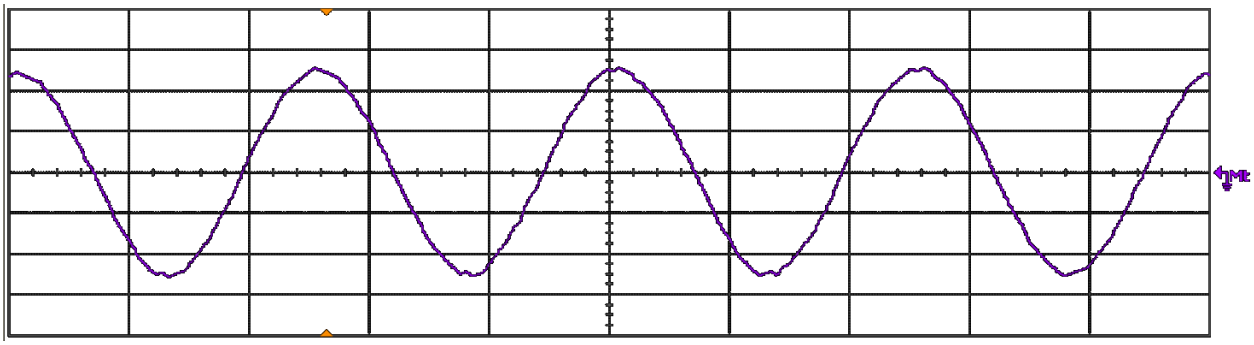


Figure 2 Calibrated jitter waveform at 25 Gbps

The SV2D is able to produce multi-UI jitter amplitudes over a range of SJ frequencies that cover various receiver CDR bandwidths. An example is illustrated in Figure 3 in which 5 UI jitter is injected at 25 Gbps. Given that most oscilloscopes are not able to recognize large jitter amounts, the measurement in the figure is made by programming a DIV10 pattern on the transmitter of the SV2D (the SV2D pattern generators are capable of creating arbitrary custom patterns).

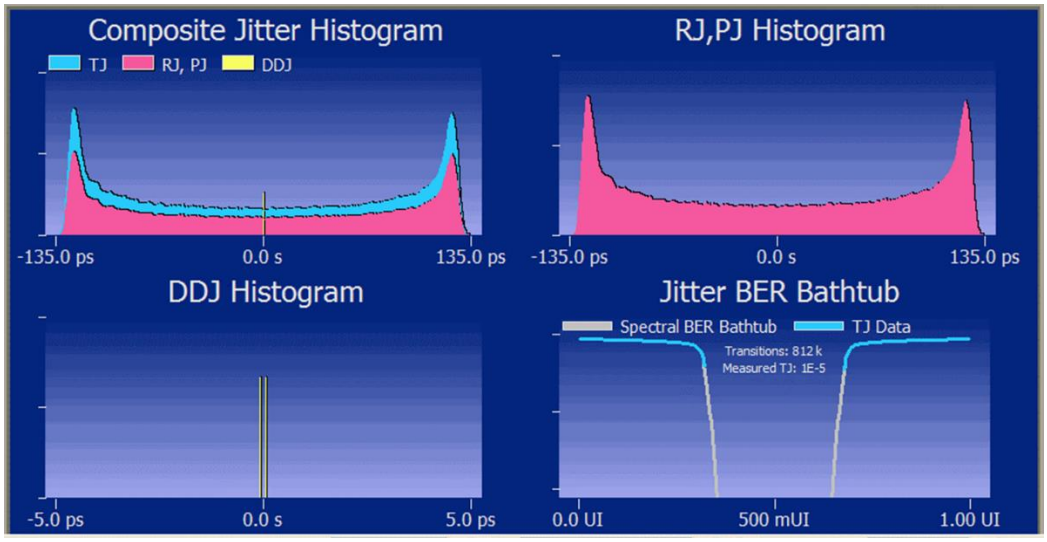


Figure 3 Multi-UI jitter injection at 25Gbps (viewed on a DIV10 pattern)

Pre-Emphasis Generation

Per-lane pre-emphasis control is integrated on the 8-lane SV2D tester. The user can individually set the transmitter pre-emphasis using a built-in Tap structure. Pre-emphasis allows the user to optimize signal characteristics at the DUT input pins.

Each transmitter in the SV2D implements a discrete-time linear equalizer as part of the driver circuit. An illustration of such equalizer is shown in Figure 4. Figure 5 shows waveform shapes with the post-tap enabled and the pre-tap enabled respectively. As can be seen, high waveform linearity is maintained even when the pre-emphasis taps are enabled. This results in superior signal integrity and more stable stressed eye generation.

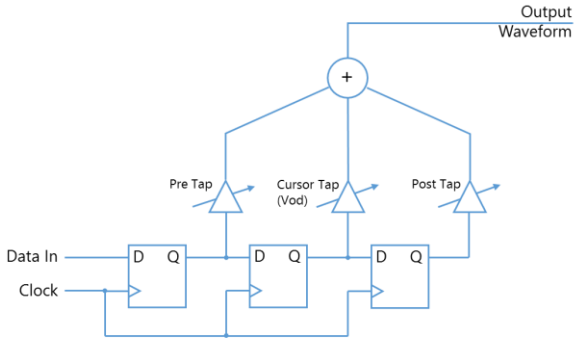
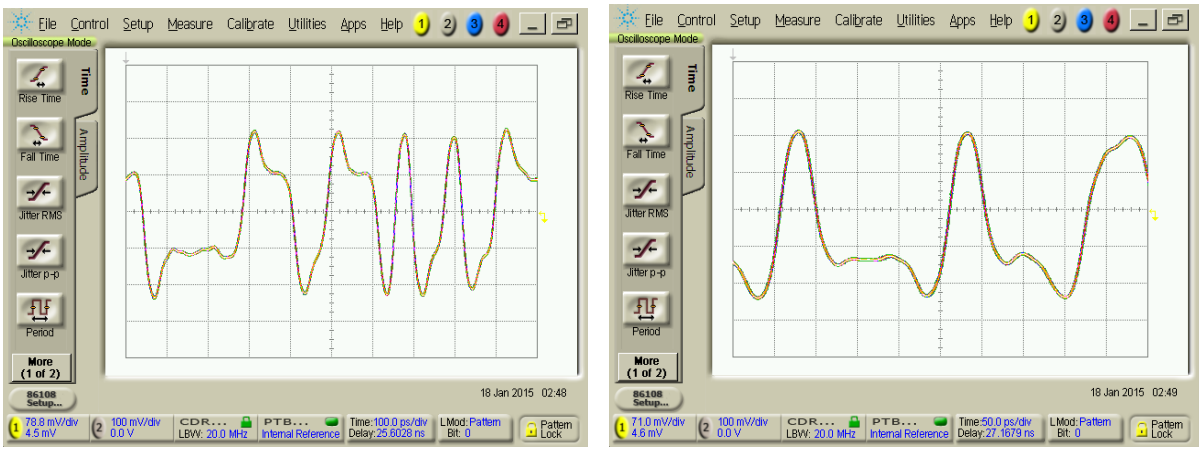


Figure 4 Illustration of pre-emphasis design



(a) *(b)*

Figure 5 Sample (a) post-tap and (b) pre-tap pre-emphasis waveforms generated by the SV2D module

Per-Lane Clock Recovery and Unique Dual-Path Architecture

In the SV2D, each receiver has its own embedded analog clock recovery circuit. Additionally, the clock recovery is monolithically integrated directly inside the receiver's high-speed sampler, thus offering the lowest possible sampling latency in a test and measurement instrument. The monolithic nature of the SV2D clock recovery helps achieve wide tracking bandwidth for measuring BER on signals that possess very high wander. Figure 6 shows a block diagram of the clock recovery capability inside the SV2D module.

Also shown in Figure 6 is the per-lane adaptive equalization design. This design is based on a continuous-time linear equalizer (CTLE), offering DC gain, broad-band gain, and high frequency gain. Such architecture allows for correcting a wide range of transmission line losses. The CTLE can be programmed to perform automatic tuning based on the test environment and the incoming data payload.

Automation

The SV2D is operated using the award winning Introspect ESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 7(a). Component-based design is Introspect ESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the software environment features automatic code generation for common tasks such as the Measurement Loop Wizard as shown in Figure 7(b).

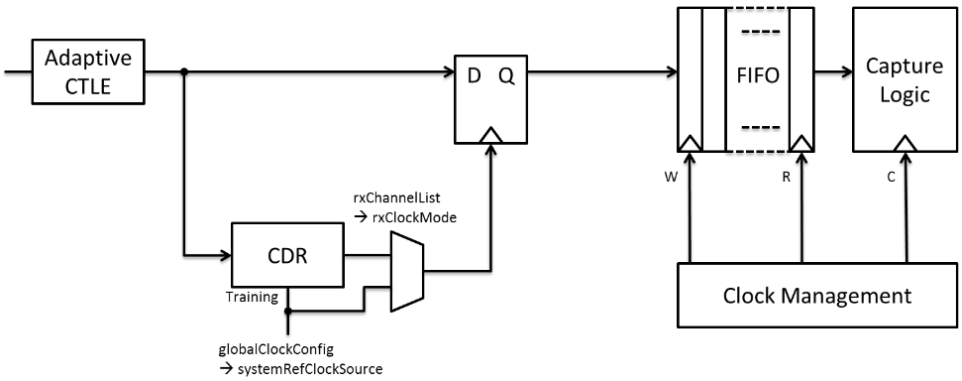
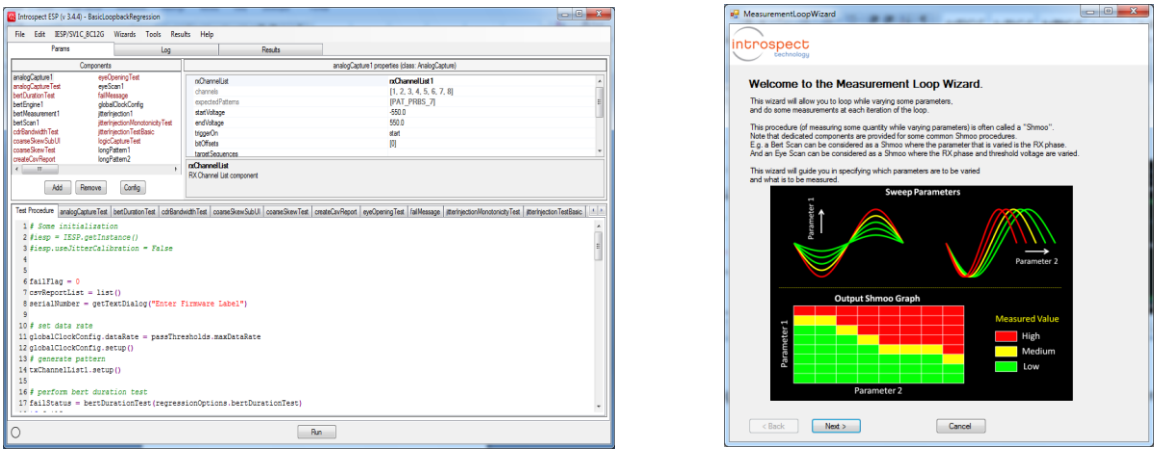


Figure 6 Per-lane clock recovery and CTLE architecture



(a) *(b)*

Figure 7 Screen capture of Introspect ESP Software user interface

Physical Description

As shown in Figure 8, the SV2D features two 16-pin MXP connectors divided into 8 pairs of RX and TX channels on top, and a 40-pin (in 20 pairs) Q Strip® connector on the bottom side for clock, JTAG and differential I/O connections with the carrier board. Pinout information is shown in Table 1, where the connections inside SV2D is illustrated in Figure 9. Figure 10 illustrates the connector coordinates and keep-out regions.

The SV2D features 5 mounting holes for physical support, and 2 holes for affixing the heat sink assembly. Figure 11 shows their dimensions and coordinates.

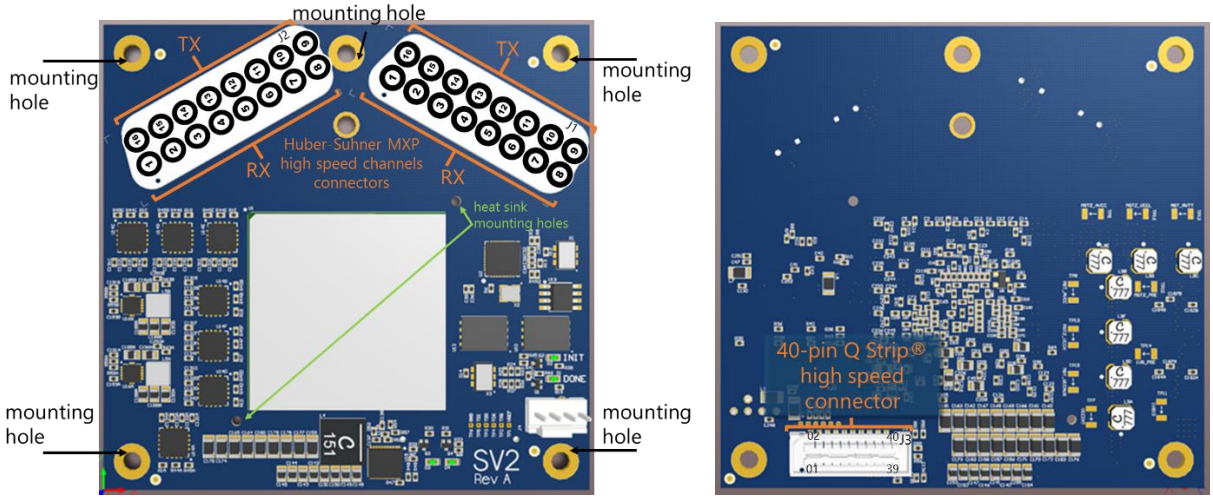
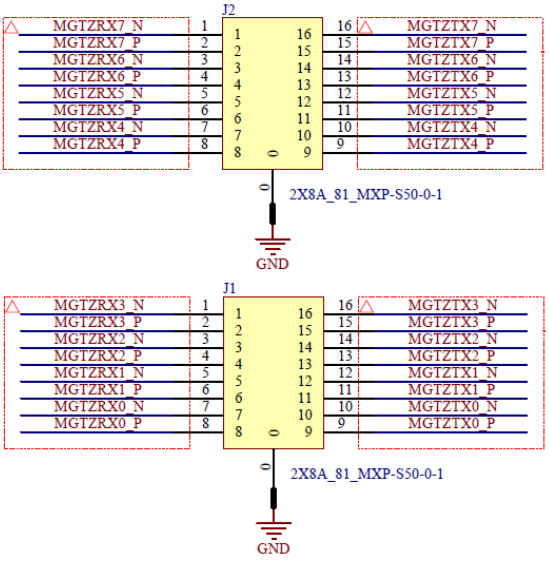


Figure 8 The (a) top and (b) bottom views of SV2D

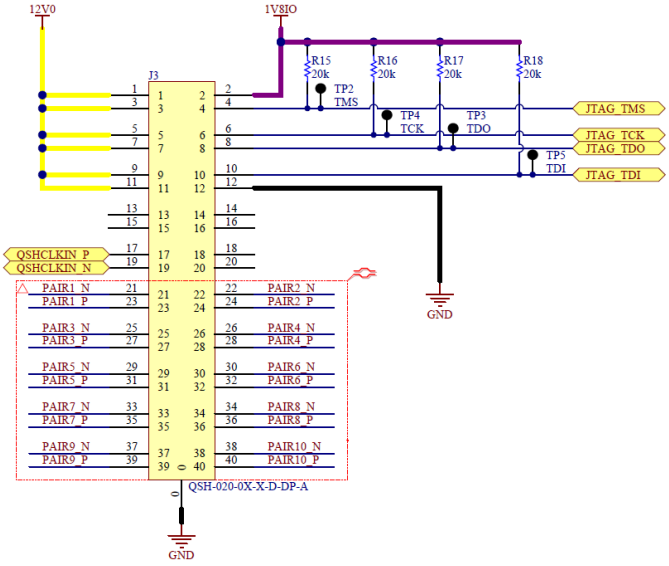
Table 1 Listing of SV2D Connectors

Port / Indicator Name	Connector Type	Component & Pin Numbers
High-Speed Transmit Channels	MXP(1)	J1, J2 pin 9-16
High-Speed Receive Channels	MXP(1)	J1, J2 pin 1-8
Differential CLK Input Pins	Q Strip® (2)	J3 pin 17, 19
JTAG Control and Data Pins	Q Strip® (2)	J3 pin 4, 6, 8, 10
Differential Pair I/O Channels	Q Strip® (2)	J3 pin 21-40

(1) Connector Part number: 2X8A_81_MXP-S50-0-1
(2) Connector Part number: QSH-020-0X-X-D-DP-A



(*a*)



(b)

Figure 9 Schematics of the MXP and Q Strip® connectors inside SV2D

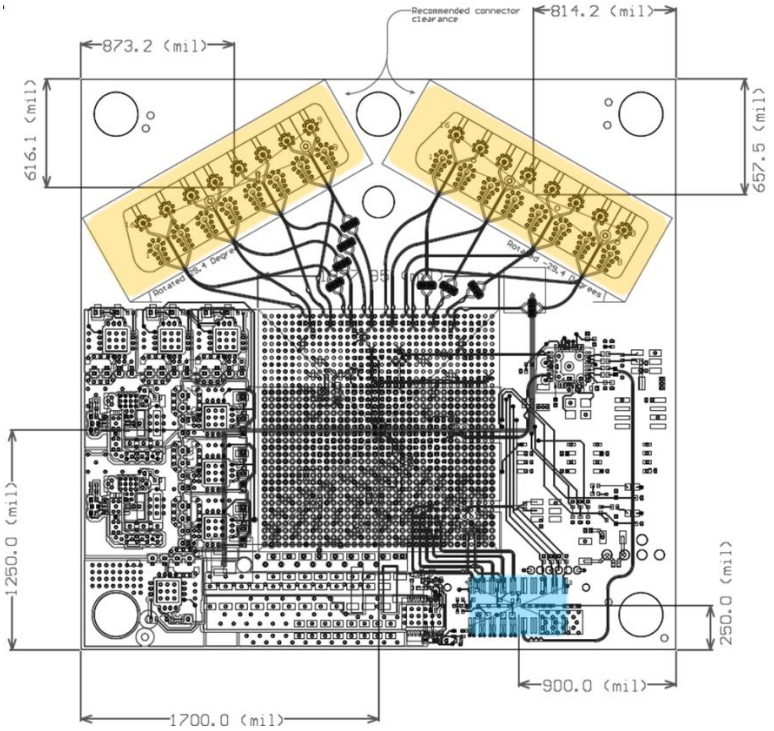


Figure 10 Physical dimensions of MXP (in yellow) and Q Strip (in blue, under-side of board) connectors

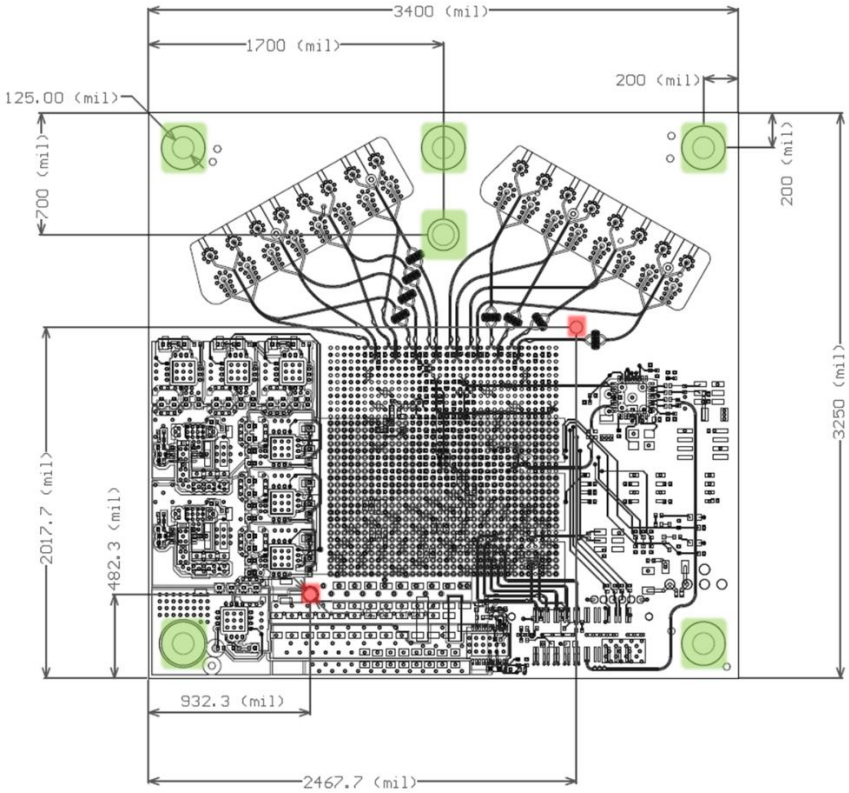


Figure 11 Physical dimensions of board (in green) and heat sink fixture (in red) mounting hole

Specifications

Table 2 General Specifications

Parameter	Value	Units	Description and Conditions
Ports			
Number of Differential Transmitters	8		
Number of Differential Receivers	8		
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input.
Data Rates and Frequencies			
Minimum Programmable Data Rate	19.6	Gbps	Contact factory for extension to lower data rates.
Maximum Programmable Data Rate	28.05	Gbps	(See Figure 12)
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Minimum External Input Clock Frequency	25	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)

Table 3 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
Output Coupling			
DC common mode voltage	1.2V – VOD/2	mV	where VOD is programmed differential swing. Operate in AC coupled mode only.
AC Output Differential Impedance	100	Ohm	Typical
Voltage Performance			
Minimum Differential Voltage Swing	600	mV	
Maximum Differential Voltage Swing	1080	mVpp	
Differential Voltage Swing Resolution	30	mV	
Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Rise and Fall Time	15	ps	Typical, 20-80% (See Figure 13)
De-emphasis Performance			
Pre-Emphasis Pre-Tap Range	0 to 4	dB	Only high-pass function available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range. Preliminary specification.
Pre-Emphasis Pre-Tap Resolution	Range / 16	dB	
Pre-Emphasis Post1-Tap Range	0 to 15	dB	Only high-pass function is available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range. Preliminary specification.
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	

Jitter Performance			
Random Jitter Noise Floor	700	fs	Preliminary specification. Measurement with DCA-X with 86108B Precision Waveform Analyzer.
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	60	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1100	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Common		Common across all channels within a unit.
Maximum RMS Random Jitter Injection	0.1	UI	
Magnitude Resolution of Injected Jitter	0.1	ps	
Accuracy of Injected Jitter Magnitude	TBD	%, ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	TBD	ps	

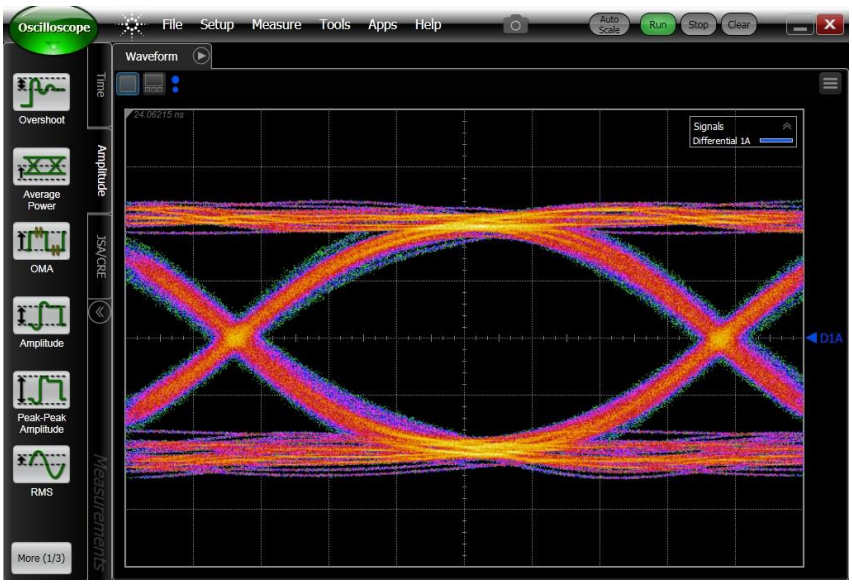


Figure 12 PRBS9 eye diagram at 28.05 Gbps

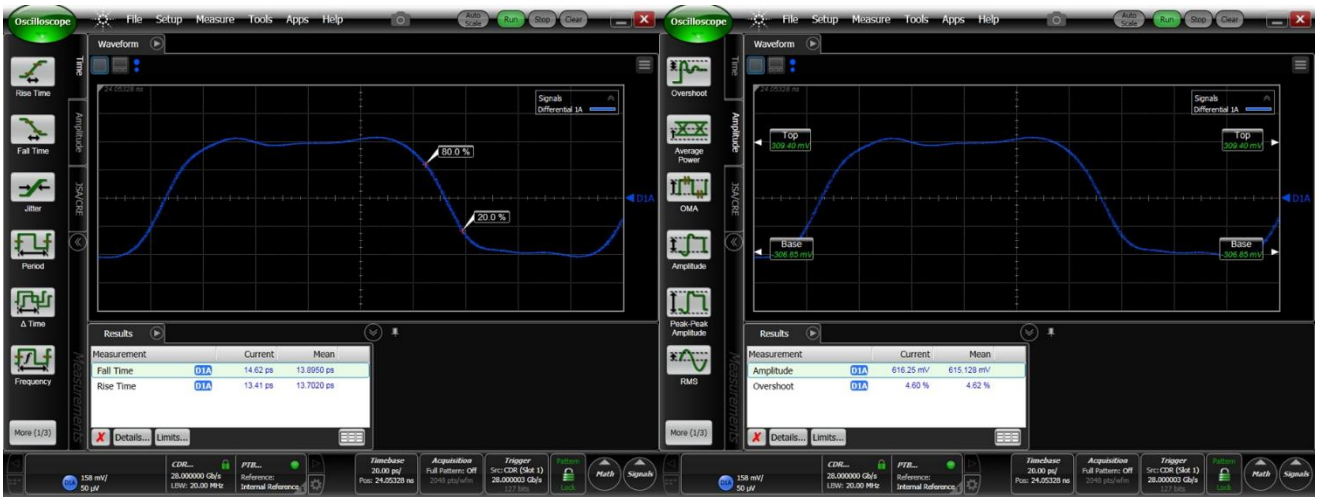


Figure 13 Typical signal waveform parameters.

Table 4 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
AC Input Differential Impedance	100	Ohm	
AC Performance			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Differential Comparator Threshold Voltage Accuracy	TBD	%, mV	
Resolution Enhancement & Equalization			
DC Gain, CTLE Gain	Automatic	dB	DC Gain and CTLE Equalization can be set to automatic optimization or can be disabled.
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		

Table 5 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	1		
Embedded Clock Applications			
Transmit Timing Modes	System Extracted		Clock can be extracted from one of the data receiver channels in order to drive all transmitter channels.
Receive Timing Modes	System Extracted		All channels have clock recovery for extracted mode operation.
Per-Lane CDR Tracking Bandwidth	Line Rate / 1667		

Table 6 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Loopback			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	Maintained across cascaded modules.
Preset Patterns			
Standard Built-In Patterns	All Zeros D21.5 K28.5 K28.7 DIV.16 DIV.20 DIV.40 DIV.50 PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.21 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
User-programmable Pattern Memory			
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	1024	bits	
Maximum Pattern Segment Size	131072	bits	
Total Memory Space for Transmitters	1	Mbits	Memory allocation is customizable. Contact factory.
Total Expected Memory Space for Receivers	1	Mbits	Memory allocation is customizable. Contact factory.
Pattern Sequencing			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	4		This refers to the number of sequencer slots that can operate at any given time. The instrument has storage space for 16 different sequencer programs.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
Additional Pattern Characteristics			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	

Table 7 Measurement and Throughput Characteristics

Parameter	Value	Units	Description and Conditions
BERT Sync			
Alignment Modes	Pattern		Module can align to any user pattern or preset pattern.
	PRBS		
Minimum SYNC Error Threshold	3	bits	
Maximum SYNC Error Threshold	2^{32}-1	bits	
Minimum SYNC Sample Count	1024	bits	
Maximum SYNC Sample Count	2^{32}	bits	
SYNC Time	20	ms	Assumes a PRBS7 pattern that is stored in a user pattern segment and worst case misalignment between DUT pattern and expected pattern; data rate is 3.25 Gbps.
BERT			
Error Counter Size	32	bits	Sample counts in the BERT are programmed in increments of 32 bits.
Maximum Single-Shot Duration	2^{32}-1	bits	Repeat mode is available to continuously count over longer durations.
Continuous Duration	Indefinite		
Alignment			
CDR Lock Time	5	us	
Self-Alignment Time	50	ms	

Table 8 Instruction Sequence Cache

Parameter	Value	Units	Description and Conditions
Simple Instruction Cache			
Instruction Learn mode Instruction	Start Stop Replay		
Advanced Instruction Cache			
Local Instruction Storage	1M Instructions		
Instruction Sequence Segments	1000		

Revision Number	History	Date
1.0	Document release	Jan 20, 2016
1.1	Spec update	April 21, 2016
1.2	Updated FFE figure	April 10, 2017

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