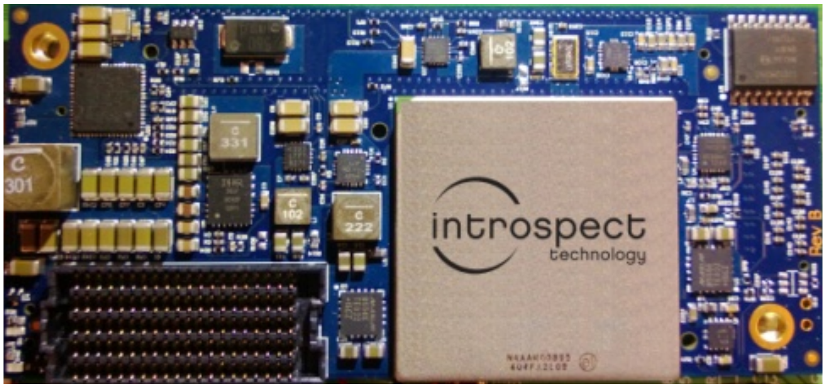
SV1D Direct-Attach SerDes Module



Data Sheet

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Introduction

Overview

The SV1D Direct-Attach SerDes Module is a versatile, high-performance instrument that creates a new category of tool for high-speed digital product engineering teams. It integrates multiple technologies in order to enable the self-contained test and measurement of complex SerDes interfaces such as PCI Express Gen 3, MIPI M-PHY, Thunderbolt, or USB3. Coupled with a seamless, easy-to-use development environment, this tool enables product engineers with widely varying skills to efficiently work with and develop SerDes verification algorithms. The SV1D mounts directly on an application or test board without cables. It contains 8 independent stimulus generation ports, 8 independent capture and measurement ports and various clocking, synchronization and lane-expansion capabilities. It has been designed specifically to address the growing need of a parallel, system-oriented test methodology while offering world-class signal-integrity features such as jitter injection and jitter measurement.

With a small footprint, an extensive signal-integrity feature set, and an exceptionally powerful software development environment, the SV1D is not only suitable for signal-integrity verification engineers that perform traditional characterization tasks, but it is also ideal for FPGA developers and software developers who need rapid turnaround signal verification tools or hardware-software interoperability confirmation tools. The SV1D integrates state of the art functions such as digital data capture, bit error rate measurement, clock recovery, jitter decomposition and jitter generation.

Key Benefits

- True parallel bit-error-rate measurement across 8 lanes
- Fully-synthesized integrated jitter injection on all lanes
- Fully-automated integrated jitter testing on all lanes
- Optimized pattern generator rise-time for receiver stress test applications
- Flexible pre-emphasis and equalization
- Flexible loopback support per lane
- Hardware clock recovery per lane
- State of the art programming environment based on the highly intuitive Python language
- Integrated device control through SPI, I2C, or JTAG
- Reconfigurable, protocol customization (on request)

Applications

Parallel PHY validation of serial bus standards such as:

- PCI Express (PCIe)
- UHS-2
- MIPI M-PHY
- CPRI
- USB
- HDMI
- Thunderbolt
- XAUI
- JESD204B
- SATA

Interface test of electrical/optical media such as:

- Backplane
- Cable
- CFP MSA, SFP MSA, SFP+ MSA

Plug-and-play system-level validation such as:

- PCI Express
- DisplayPort sink/source
- MIPI M-PHY

Timing verification:

- PLL transfer function measurement
- Clock recovery bandwidth verification
- Frequency ppm offset characterization

Mixed-technology applications:

- High-speed ADC and DAC (JESD204) data capture and/or synthesis
- FPGA-based system development
- Channel and device emulation

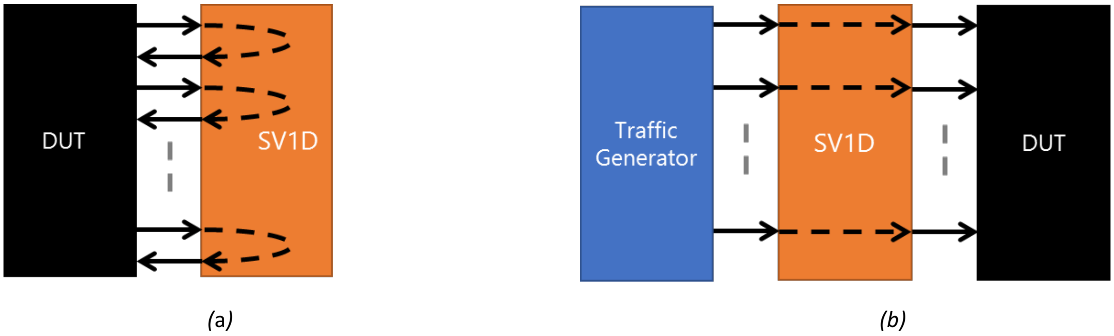
Features

Multi-Lane Loopback

The SV1D is the only bench-top tool that offers instrument-grade loopback capability on all differential lanes. The loopback capability of the SV1D includes:

- Retiming of data for the purpose of decoupling DUT receiver performance from DUT transmitter performance
- Arbitrary jitter or voltage swing control on loopback data

Figure 1 shows two common loopback configurations that can be used with the SV1D. In the first configuration, a single DUT's transmitter and receiver channels are connected together through the SV1D. In the second configuration, arbitrary pattern testing can be performed on an end-to-end communications link. The SV1D is used to pass data through from a traffic generator (such as an end-point on a real system board) to the DUT while stressing the DUT receiver with jitter, skew, or voltage swing.



(a) (b)

Figure 1 Illustration of loopback applications

Multiple-Source Jitter Injection

The SV1D is capable of generating calibrated jitter stress on any data pattern and any output lane configuration. Sinusoidal jitter injection is calibrated in the time and frequency domain in order to generate high-purity stimulus signals as shown in Figure 2.

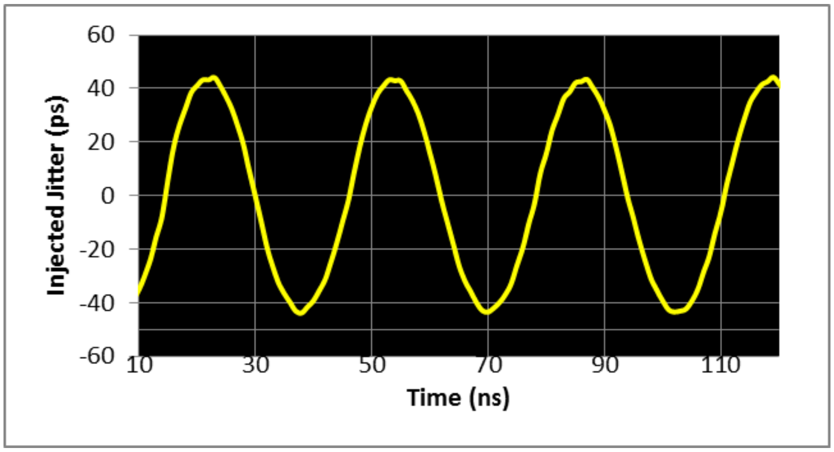
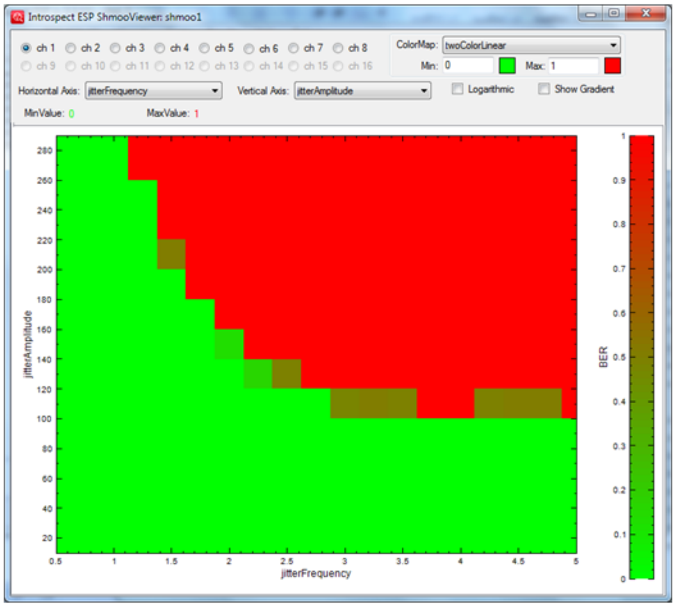


Figure 2 Illustration of calibrated jitter waveform

The jitter injection feature is typically exploited to perform automated jitter tolerance testing as shown in the example in Figure 3. As is the case for other features in the SV1D Direct-Attach SerDes Module, jitter tolerance testing is conducted in parallel across all lanes. For advanced applications, the SV1D also includes RJ injection and a third-source arbitrary waveform jitter synthesizer.


Introspect ESP ShmooViewer: shmoo1

● ch 1 ○ ch 2 ○ ch 3 ○ ch 4 ○ ch 5 ○ ch 6 ○ ch 7 ○ ch 8
○ ch 9 ○ ch 10 ○ ch 11 ○ ch 12 ○ ch 13 ○ ch 14 ○ ch 15 ○ ch 16

ColorMap: twoColorLinear
Min: 0 🟩 Max: 1 🟥
Horizontal Axis: jitterFrequency
Vertical Axis: jitterAmplitude
☐ Logarthmic ☐ Show Gradient
MinValue: 0 MaxValue: 1

Figure 3 Illustration of jitter tolerance curve

Pre-Emphasis Generation

Conventionally offered as a separate instrument, per-lane pre-emphasis control is integrated on the 8-lane SV1D tester. The user can individually set the transmitter pre-emphasis using a built-in Tap structure. Pre-emphasis allows the user to optimize signal characteristics at the DUT input pins.

Each transmitter in the SV1D implements a discrete-time linear equalizer as part of the driver circuit. An illustration of such equalizer is shown in Figure 4, and sample synthesized waveform shapes are shown in Figure 5.

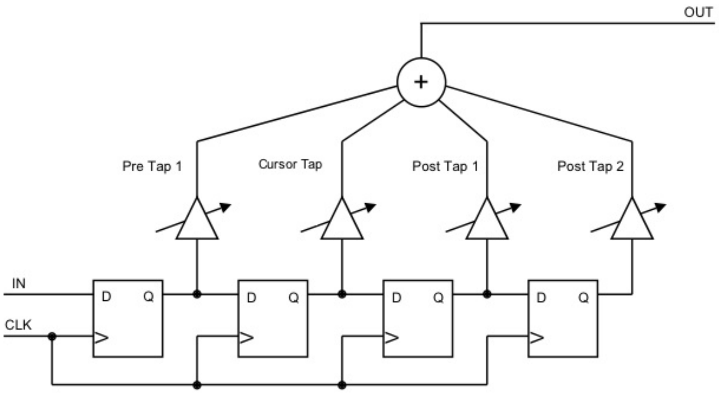
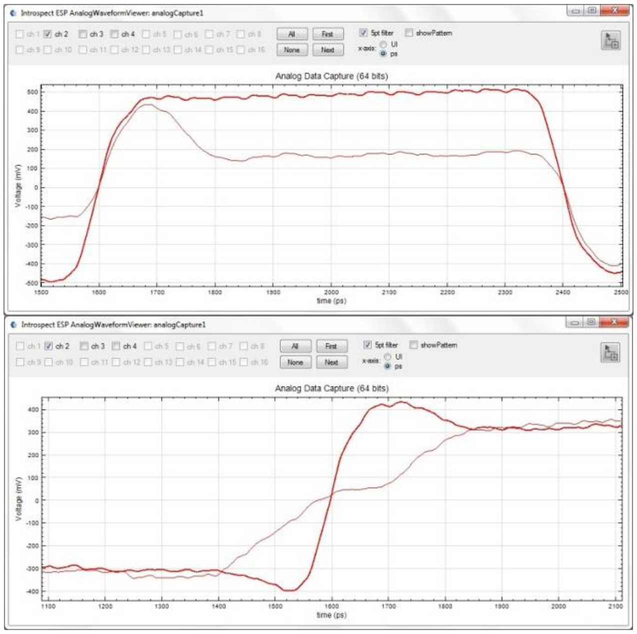


Figure 4 Illustration of pre-emphasis design


Introspect ESP AnalogWaveformViewer: analogCapture1

☐ ch 1 ☑ ch 2 ☐ ch 3 ☐ ch 4 ☐ ch 5 ☐ ch 6 ☐ ch 7 ☐ ch 8
☐ ch 9 ☐ ch 10 ☐ ch 11 ☐ ch 12 ☐ ch 13 ☐ ch 14 ☐ ch 15 ☐ ch 16
☑ 5pt filter ☐ showPattern
x-axis: ○ UI ● ps

Introspect ESP AnalogWaveformViewer: analogCapture1

☐ ch 1 ☑ ch 2 ☐ ch 3 ☐ ch 4 ☐ ch 5 ☐ ch 6 ☐ ch 7 ☐ ch 8
☐ ch 9 ☐ ch 10 ☐ ch 11 ☐ ch 12 ☐ ch 13 ☐ ch 14 ☐ ch 15 ☐ ch 16
☑ 5pt filter ☐ showPattern
x-axis: ○ UI ● ps

Figure 5 Illustration of multiple waveform shapes that can be synthesized using the pre-emphasis function of the SV1D

Programmable SSC Generation and Frequency Synthesis

The SV1D incorporates precision frequency synthesis technology that allows for the generation of programmable SSC waveforms at any data rate. The SSC waveforms are superimposed on the pattern generator outputs, and they coexist with other jitter injection sources of the SV1D. Thus, a truly complete jitter cocktail can be produced for the most thorough receiver validation. Figure 6 illustrates the SSC capability of the SV1D. In the figure, the SV1D is programmed to synthesize four slightly different modulation frequencies showcasing the precision programmability of the tool.

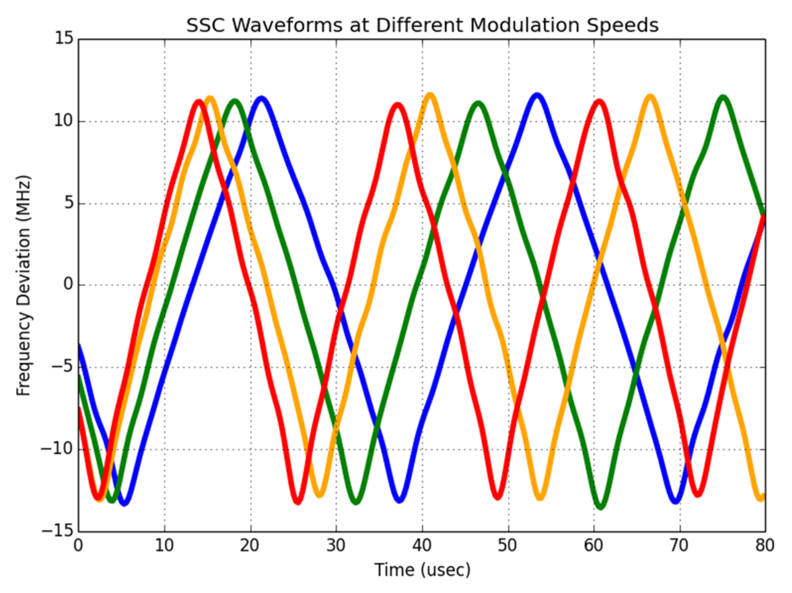


Figure 6 Programmable SSC generation

Per-Lane Clock Recovery and Unique Dual-Path Architecture

Like pre-emphasis, conventional tools often require separate clock recovery instrumentation. In the SV1D, each receiver has its own embedded analog clock recovery circuit. Additionally, the clock recovery is monolithically integrated directly inside the receiver's high-speed sampler, thus offering the lowest possible sampling latency in a test and measurement instrument. The user does not have to make special connections or carefully match cable lengths. The monolithic nature of the SV1D clock recovery helps achieve wide tracking bandwidth for measuring signals that possess spread-spectrum clocking or very high amplitude wander. Figure 7 shows a block diagram of the clock recovery capability inside the SV1D Direct-Attach SerDes Module.

Also shown in Figure 7 is the dual-path receiver architecture of the SV1D. This unique architecture allows the SV1D to operate as both a digital capture/analysis instrument and an analog measurement instrument. A feature rich clock management system allows for customization of the SV1D to specific customer requirements.

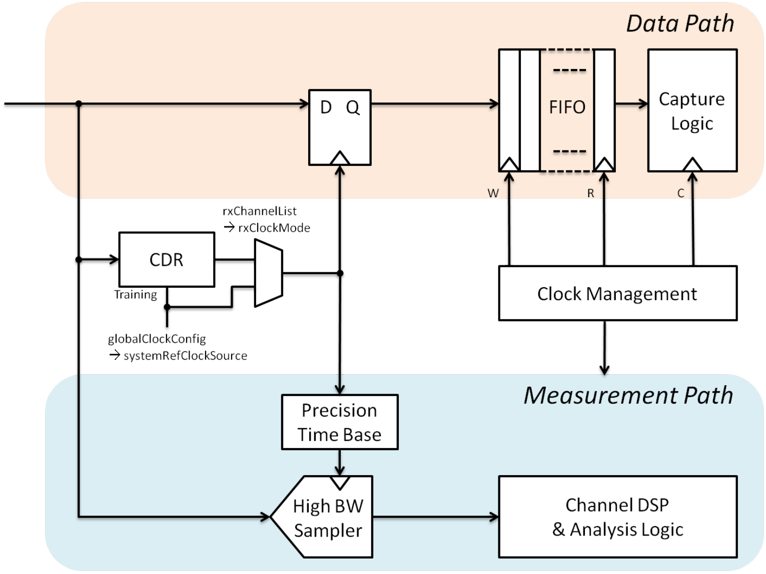


Figure 7 Per-lane clock recovery and dual-path architecture

Auxiliary Control Port

The SV1D includes a low-speed auxiliary control port. It enables controlling DUT registers through JTAG, I2C, or SPI. Additionally, the port includes reconfigurable trigger and flag capabilities for synchronizing with external tools or events.

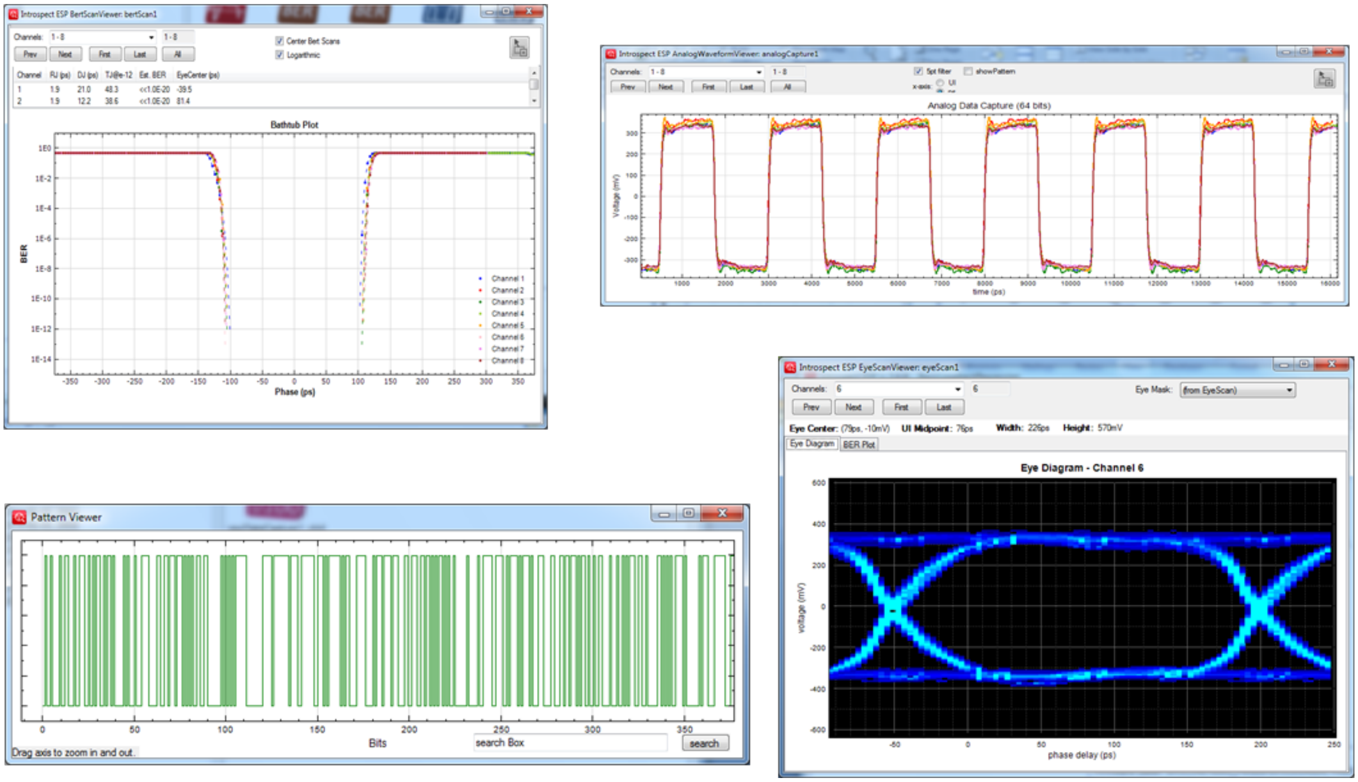
Analysis

The SV1D instrument has an independent Bit Error Rate Tester (BERT) for each of its input channels. Each BERT compares recovered (retimed) data from a single input channel against a specified data pattern and reports the bit error count.

Apart from error counting, the instrument offers a wide range of measurement and analysis features including:

- Jitter separation
- Eye mask testing
- Voltage level, pre-emphasis level, and signal parameter measurement
- Frequency measurement and SSC profile extraction

Figure 8 illustrates a few of the analysis and reporting features of the SV1D. Starting from the top left and moving in a clock-wise manner, the figure illustrates bathtub acquisition and analysis, waveform capture, raw data viewing, and eye diagram plotting. As always, these analysis options are executed in parallel on all activated lanes.



Channels: 1 - 8 | 1 - 8

☑ Center Bert Scans
☑ Logarithmic

Channel	RJ (ps)	DJ (ps)	TJ@e-12	Est. BER	EyeCenter (ps)
1	1.9	21.0	48.3	<<1.0E-20	-39.5
2	1.9	12.2	38.6	<<1.0E-20	81.4

Channels: 1 - 8 | 1 - 8

☑ Spt filter ☐ showPattern

Channels: 6 | 6

Eye Mask: (from EyeScan)

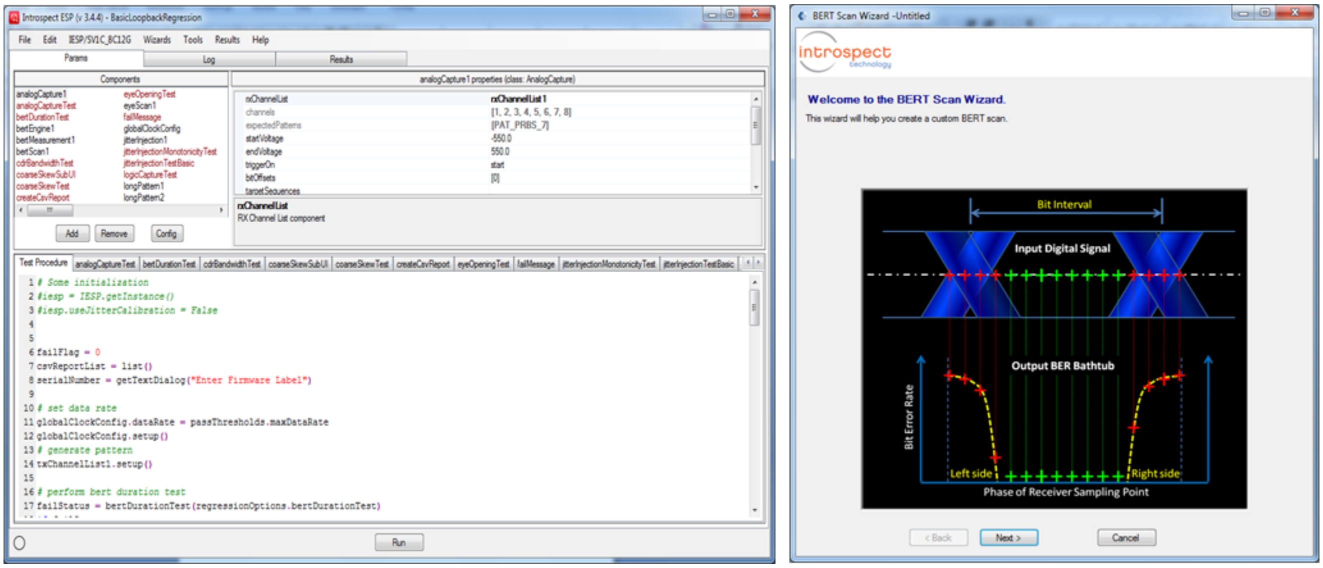
Eye Center: (79ps, -10mV) **UI Midpoint:** 76ps **Width:** 226ps **Height:** 570mV

search Box

Figure 8 Sampling of analysis and report windows

Automation

The SV1D is operated using the award winning IntrospectESP Software. It features a comprehensive scripting language with an intuitive component-based design as shown in the screen shot in Figure 9(a). Component-based design is IntrospectESP's way of organizing the flexibility of the instrument in a manner that allows for easy program development. It highlights to the user only the parameters that are needed for any given task, thus allowing program execution in a matter of minutes. For further help, the SV1D features automatic code generation for common tasks such as Eye Diagram or Bathtub Curve generation as shown in Figure 9(b).



rxChannelList	rxChannelList1
channels	[1, 2, 3, 4, 5, 6, 7, 8]
expectedPatterns	[PAT_PRBS_7]
startVoltage	-550.0
endVoltage	550.0
triggerOn	start
bitOffsets	[0]
targetSequences	

rxChannelList
RX Channel List component

```
# Some initialization
#iesp = IESP.getInstance()
#iesp.useJitterCalibration = False


failFlag = 0
csvReportList = list()
serialNumber = getTextDialog("Enter Firmware Label")

# set data rate
globalClockConfig.dataRate = passThresholds.maxDataRate
globalClockConfig.setup()
# generate pattern
txChannelList1.setup()

# perform bert duration test
failStatus = bertDurationTest(regressionOptions.bertDurationTest)
```

Welcome to the BERT Scan Wizard.

This wizard will help you create a custom BERT scan.

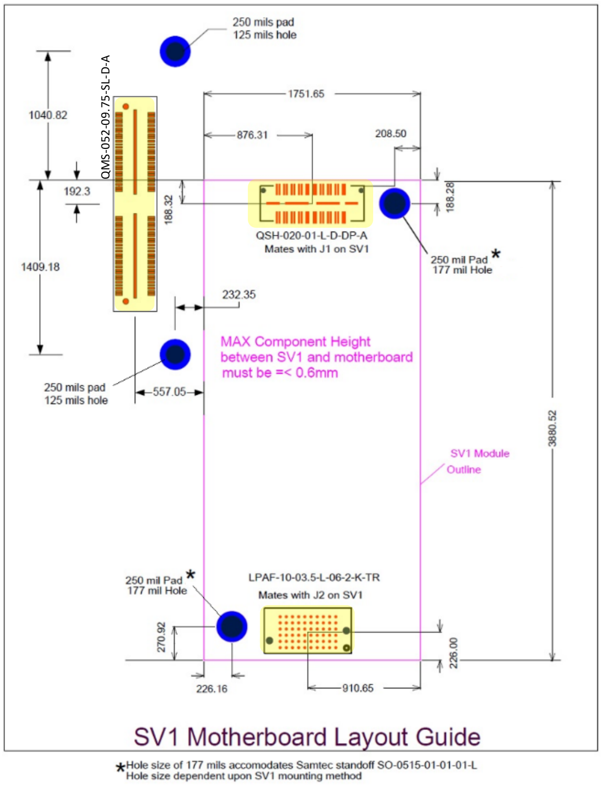
(a) *(b)*

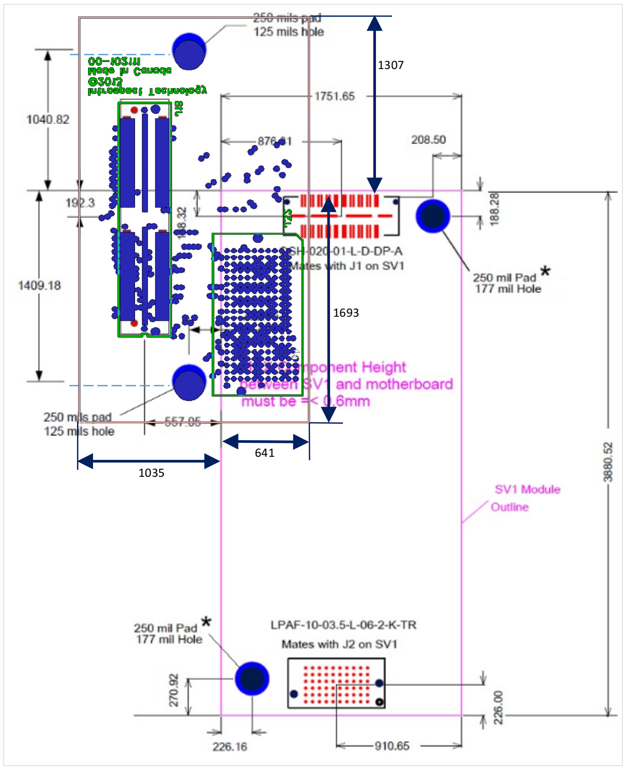
Figure 9 Screen capture of IntrospectESP user environment.

Physical Description

The SV1D is supplied with a heatsink and the SV1B adaptor board. The motherboard and its connectors, standoffs and screws are to be sourced by users. The SV1D features a high-speed low profile 6x10-pin and a 40-pin (in 20 pairs) Q-Strip® connectors on the bottom side providing clock, data, SPI, JTAG control connections to the carrier motherboard. A connector on upper side provides GPIO connections to the motherboard through the included SV1B adaptor board.

Figure 10(a) illustrates the 3 connector and 4 mounting hole locations required on the motherboard. Measurements are in *mil* unless stated otherwise. The SV1D and SV1B boards require 2 mounting holes each for physical support. The motherboard devices should be kept away from the locations occupied by SV1D and SV1B, as shown in Figure 10(b).





ıe connector and mounting hole footprints of the SV1D (pink outline)

(a)

(b)

(b) Top view of the SV1B adaptor board location (brown outline) relative to the SV1D

The side profile of the assembled boards is shown in Figure 11, where the SV1D is mounted on the motherboard first, and then the SV1B board mounts on top of it. Please take note of the length of the standoffs needed to maintain adequate vertical clearance and tight connections among the SV1D, SV1B and the motherboard. The standoffs should be tightened by screws after assembly.

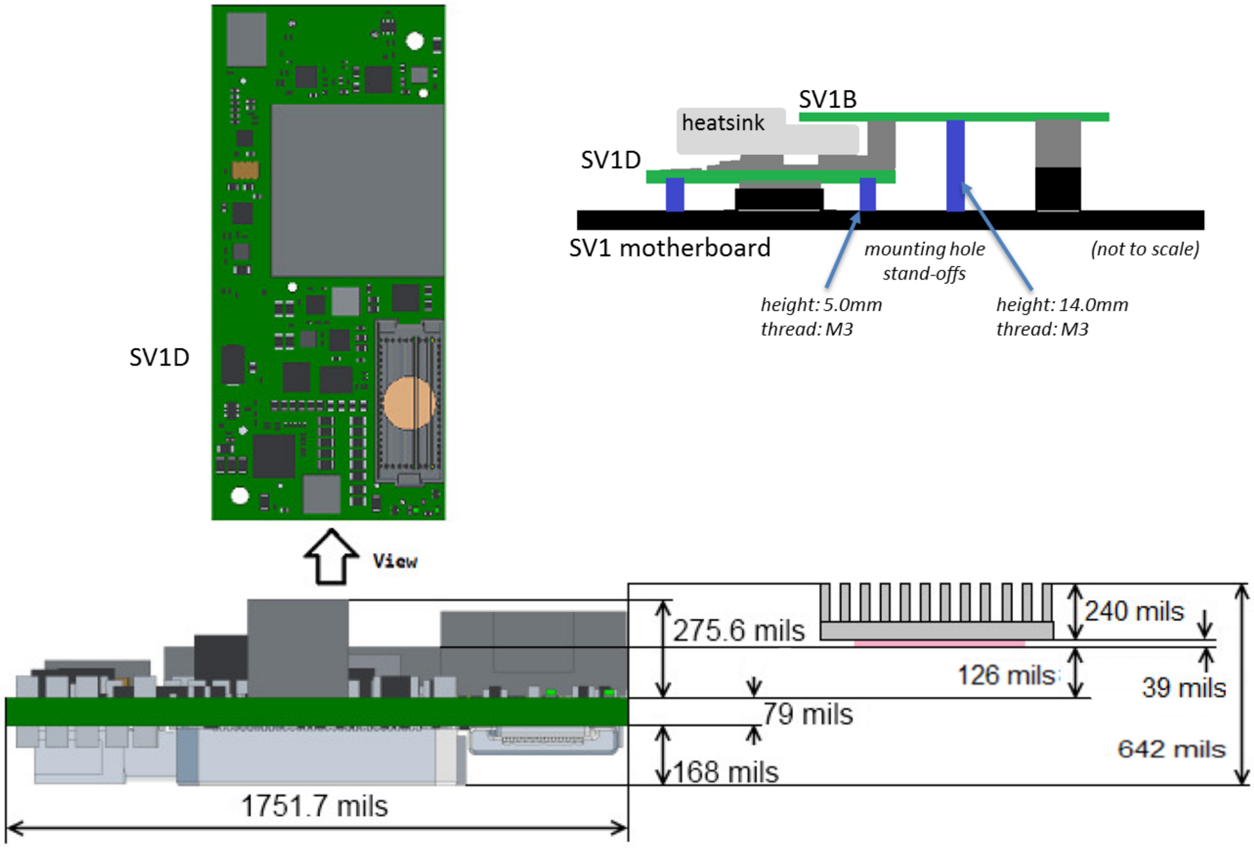


Figure 11 Top view and side profile of the SV1M showing its relief and the total height with the included heat sink
Inset figure depicts the side view of the assembled SV1B, SV1D and the motherboard

Electrical Description

The following tables describes the pin out information of the 2 Q-strip connectors on the SV1D, and the IO connector on the motherboard. When designing the interface logic, please ensure not to drive any I/O pins on the SV1D until the power rails have been completely powered on.

Table 1 Motherboard J1 connector QSH-020-01-L-D-DP-A pin-out

Signal	Pin Location	Description	Voltage Level
12.0V	10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40	Input Power (12.0V +/- 5% at ALL times) (Current source minimum 2A, application may demand more)	12.0V
GND	0,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39	Ground	GND
TMS	9	JTAG TMS | Direct connection to FPGA	2.5V
SCLK	1	SV1D slave SPI communication port clock	
SSN	3	SV1D slave SPI communication port chip select | Active low	
MOSI	5	SV1D slave SPI communication port data from master	
MISO	7	SV1D slave SPI communication port data to master |Open drain output	
TRIG1	2	Multi-purpose Trigger input | Negative edge triggered	
TRIG2	4		
FLAG1	6	Multi-purpose Flag output	
FLAG2	8		

Table 2 Motherboard J2 connector LPAF-10-03.5-L-06-2-K-TR pin-out

Signal	Pin Location	Description	Voltage Level
REFCLK_0_P, REFCLK_0_N	F02, E02	External Reference Clock | LVDS | AC Coupled Refer to connection diagrams	GXB
TX8_P, TX8_N	B03, A03	GXB Transmit Link | DC coupled | Programmable voltage swing	
TX7_P, TX7_N	C04, B04		
TX6_P, TX6_N	B05, A05		
TX5_P, TX5_N	C06, B06		
TX4_P, TX4_N	B07, A07		
TX3_P, TX3_N	C08, B08		
TX2_P, TX2_N	B09, A09		
TX1_P, TX1_N	C10, B10		
RX8_P, RX8_N	E03, D03	GXB Receive Link | DC coupled	
RX7_P, RX7_N	F04, E04		
RX6_P, RX6_N	E05, D05		
RX5_P, RX5_N	F06, E06		
RX4_P, RX4_N	E07, D07		
RX3_P, RX3_N	F08, E08		
RX2_P, RX2_N	E09, D09		
RX1_P, RX1_N	E10, F10		
SV1_RST#	B02	Resistor divider on SV1 makes 3.3V SV1_RST# signal 2.5V compatible | Active low | Must be actively driven or pulled up with a resistor smaller than 1Kohms	3.3V
REFCLK_1_P	B01	External Reference Clock | Expected to be 100MHz LVDS_2.5V zczxcv|)Motherboard Refer to connection diagrams	2.5V LVDS
REFCLK_1_N	A01		2.5G LVDS
TDO	C02	JTAG TDO | Direct connection to FPGA	2.5V
TDI	E01	JTAG TDI | Direct connection to FPGA	
TCK	D01	JTAG TCK | Direct connection to FPGA	
GND	A02,A04,A06,A08,A10, C01,C03,C05,C07,C09, D02,D04,D06,D08,D10, F01,F03,F05,F07,F09	Ground	GND

Table 3 Motherboard J4 connector QMS-052-09.75-SL-D-A pin-out

Signal	Pin Location	Description	Voltage Level
PAIR00_P, PAIR00_N	1, 2	Generic IO, Programmable with Custom Firmware	2.5 V CMOS
12.0V	3,4	Output Power (12.0V +/- 5%)	12.0V
PAIR04_P, PAIR04_N	5, 6	LED: Lock Status, CmdProcReady	2.5V
PAIR02_P, PAIR02_N	13, 14	LED: Lock Status, CmdProcReady	2.5V
PAIR08_P, PAIR08_N	9, 10	Generic IO, Programmable with Custom Firmware	2.5 V CMOS
PAIR06_P, PAIR06_N	17, 18		
PAIR01_P, PAIR01_N	21, 22	LED: User LED mirror, LED: Lock Status mirror	
PAIR05_P, PAIR05_N	25, 26	Generic IO, Programmable with Custom Firmware	
PAIR09_P, PAIR09_N	29, 30		
PAIR03_P, PAIR03_N	33,34		
PAIR07_P, PAIR07_N	37, 38		
GND	7,8,11,12,15,16,19,20,23,24,27,28,31,32,35,36,39,40,43,44,47,48,51,52,55,56,59,60,63,64,67,68,71,72,75,76,79,80,83,84,87,88,91,92,95,96,99,100,103,104,107,108,111,112,115,116,119,120,123,124,127,128,131,132,135,136,139,140,143,144,147,148,151,152,155,156,159,160,163,164,167,168,171,172,175,176,179,180,183,184,187,188191,192,195,196,199,200	Ground	GND
PAIR10_P, PAIR10_N	41, 42	Generic IO, Programmable with Custom Firmware	2.5 V CMOS
PAIR14_P, PAIR14_N	45, 46		
PAIR18_P, PAIR18_N	49, 50		
PAIR12_P, PAIR12_N	53, 54		
PAIR16_P, PAIR16_N	57, 58		
PAIR11_P, PAIR11_N	61, 62		
PAIR15_P, PAIR15_N	65, 66		
PAIR19_P, PAIR19_N	69, 70		
PAIR13_P, PAIR13_N	73, 74		
PAIR17_P, PAIR17_N	77, 78		
PAIR20_P, PAIR20_N	81, 82		
PAIR24_P, PAIR24_N	85, 86	DUT reset (active low, driven low or high-z, pull-up	
PAIR28_P, PAIR28_N	89, 90	Generic IO, Programmable with Custom Firmware	
PAIR22_P, PAIR22_N	93, 94		
PAIR26_P, PAIR26_N	97, 98		
PAIR21_P, PAIR21_N	101, 102		
PAIR25_P, PAIR25_N	105, 106		
PAIR29_P, PAIR29_N	109, 110		
PAIR23_P, PAIR23_N	113, 114		
PAIR27_P, PAIR27_N	117, 118		
PAIR30_P, PAIR30_N	121, 122		
PAIR45_P, PAIR45_N	125, 126		
PAIR34_P, PAIR34_N	129, 130		
MGT_RX0_P, MGT_RX0_N	133, 134	Unused input, tie to Ground	
PAIR36_P, PAIR36_N	137, 138	Generic IO, Programmable with Custom Firmware	
PAIR31_P, PAIR31_N	141, 142		
PAIR38_P, PAIR38_N	145, 146		
PAIR42_P, PAIR42_N	149, 150		
MGT_RX1_P, MGT_RX1_N	153, 154	Unused input, tie to Ground	
PAIR40_P, PAIR40_N	157, 158	Generic IO, Programmable with Custom Firmware	
PAIR32_P, PAIR32_N	161, 162		
PAIR44_P, PAIR44_N	165, 166		
PAIR35_P, PAIR35_N	169, 170		
MGT_TX0_P, MGT_TX0_N	173, 174	Unused output, leave unconnected	
PAIR37_P, PAIR37_N	177, 178	Generic IO, Programmable with Custom Firmware	
PAIR33_P, PAIR33_N	181, 182		
PAIR39_P, PAIR39_N	185, 186		
PAIR43_P, PAIR43_N	189, 190		
MGT_TX1_P, MGT_TX1_N	193, 194	Unused output, leave unconnected	
PAIR41_P, PAIR41_N	197, 198	Generic IO, Programmable with Custom Firmware	

Specifications

Table 4 General Specifications

Parameter	Value	Units	Description and Conditions
Ports			
Number of Differential Transmitters	8		
Number of Differential Receivers	8		
Number of Dedicated Clock Outputs	2		Individually synthesized frequency and output format.
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input.
Number of Trigger Input Pins	Multiple		Consult user manual for included capability. Contact factory for customization.
Number of Flag Output Pins	Multiple		Consult user manual for included capability. Contact factory for customization.
Data Rates and Frequencies			
Minimum Programmable Data Rate	312.5	Mbps	Contact factory for extension to lower data rates.
Maximum Programmable Data Rate	14	Gbps	
Maximum Data Rate Purchase Options	4	Gbps	
	8.5	Gbps	
	12.5	Gbps	
	14	Gbps	
Data Rate Field Upgrade	4-12.5	Gbps	Contact factory for details.
Frequency Resolution of Programmed Data Rate	1	kHz	Finer resolution is possible. Contact factory for customization.
Minimum External Input Clock Frequency	25	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)

Table 5 Transmitter Characteristics

Parameter	Value	Units	Description and Conditions
Output Coupling			
DC common mode voltage	750	mV	typical (different offsets are firmware programmable)
AC Output Differential Impedance	100	Ohm	typical
Voltage Performance			
Minimum Differential Voltage Swing	20	mV	
Maximum Differential Voltage Swing	1000	mVpp	312.5 Mbps to 5 Gbps, 50 ohm AC coupled termination.
	800	mVpp	5 Gbps to 12.5 Gbps, 50 ohm AC coupled termination.
Differential Voltage Swing Resolution	20	mV	
Accuracy of Differential Voltage Swing	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Rise and Fall Time	50	ps	Typical, 500 mVpp signal, 20-80%, 50 ohm AC coupled termination.
	75	ps	Typical, 500 mVpp signal, 10%-90%, 50 ohm AC coupled termination.
Pre-emphasis Performance			
Pre-Emphasis Pre-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Pre-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post1-Tap Range	0 to 6	dB	Only high-pass function is available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post1-Tap Resolution	Range / 32	dB	
Pre-Emphasis Post2-Tap Range	-4 to +4	dB	Both high-pass and low-pass functions are available. This is the smallest achievable range based on worst-case conditions. Typical operating conditions result in wider pre-emphasis range.
Pre-Emphasis Post2-Tap Resolution	Range / 32	dB	
Jitter Performance			
Random Jitter Noise Floor	1000	fs	Based on measurement with high-bandwidth scope and with first-order clock recovery.
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Frequency of Injected Deterministic Jitter	80	MHz	
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	Contact factory for further customization.
Maximum Peak-to-Peak Injected Deterministic Jitter	1400	ps	This specification is separate from low-frequency wander generator and SSC generator.
Magnitude Resolution of Injected Deterministic Jitter	500	fs	Jitter injection is based on multi-resolution synthesizer, so this number is an effective resolution. Internal synthesizer resolution is defined in equivalent number of bits.
Injected Deterministic Jitter Setting	Per-bank		Common across all channels within a bank.
Maximum RMS Random Jitter Injection	0.1	UI	

Magnitude Resolution of Injected Jitter	0.1	ps	
Accuracy of Injected Jitter Magnitude	larger of: +/-10% of programmed value, and +/-10 ps	%, ps	
Injected Random Jitter Setting	Common		Common across all channels within a bank.
Transmitter-to-Transmitter Skew Performance			
Lane to Lane Integer-UI Minimum Skew	-20	UI	
Lane to Lane Integer-UI Maximum Skew	20	UI	
Effect of Skew Adjustment on Jitter Injection	None		
Lane to Lane Skew	+/- 30	ps	

Table 6 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
AC Input Differential Impedance	100	Ohm	
AC Performance			
Minimum Detectable Differential Voltage	25	mV	
Maximum Allowable Differential Voltage	2000	mV	
Minimum Programmable Comparator Threshold Voltage	-550	mV	
Maximum Programmable Comparator Threshold Voltage	+550	mV	
Differential Comparator Threshold Voltage Resolution	10	mV	
Differential Comparator Threshold Voltage Accuracy	larger of: +/-10% of programmed value, and +/-10mV	%, mV	
Measured Eye Width Accuracy	10%		Maximum error, 312.5 Mbps – 2.0 Gbps, 200 mVpp minimum input amplitude
	15%		Maximum error, 2.0 Mbps - 5 Gbps, 200 mVpp minimum input amplitude
	25%		Maximum error, 5 Gbps – 12.5 Gbps, 200 mVpp minimum input amplitude
Resolution Enhancement & Equalization			
DC Gain	0	dB	
	2	dB	
	4	dB	
	6	dB	
	8	dB	
CTLE Maximum Gain	16	dB	
CTLE Resolution	1	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		

Jitter Performance			
Input Jitter Noise Floor in System Reference Mode	25	ps	
Input Jitter Noise Floor in Extracted Clock Mode	10	ps	
Timing Generator Performance			
Resolution at Maximum Data Rate	31.25	mUI	Resolution (as a percentage of UI) improves for lower data rate. Contact factory for details.
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		
Skew			
Lane to Lane Skew Measurement Accuracy	+/- 10	ps	

Table 7 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	2		Relevant for future customization.
Embedded Clock Applications			
Transmit Timing Modes	System		
	Extracted		Clock can be extracted from one of the data receiver channels in order to drive all transmitter channels.
Receive Timing Modes	System		
	Extracted		All channels have clock recovery for extracted mode operation.
Lane to Lane Tracking Bandwidth	4	MHz	
Single-Lane CDR Tracking Bandwidth	3 - 12	MHz	
Forwarded Clock Applications			
Transmit Timing Modes	System		
	Forwarded		Channel 1 acts as forwarded clock for samplers.
Receive Timing Modes	System		
	Forwarded		Channel 1 acts as forwarded clock for samplers.
Clock Tracking Bandwidth	4	MHz	Second order critically damped response.
Spread Spectrum Support			
Receive Lanes Track SSC Data	Yes		Requires operation in extracted clock mode.
Transmit Lanes Generate SSC Data	Yes		Consult factory for availability.
Minimum Spread	0.1	%	
Maximum Spread	2	%	
Spread Programming Resolution	0.01	%	
Minimum Spreading Frequency	31.5	kHz	
Maximum Spreading Frequency	63	kHz	

Table 8 Pattern Handling Characteristics

Parameter	Value	Units	Description and Conditions
Loopback			
Rx to Tx Loopback Capability	Per channel		
Lane to Lane Latency Mismatch	0	UI	
Preset Patterns			
Standard Built-In Patterns	All Zeros D21.5 K28.5 K28.7 DIV.16 DIV.20 DIV.40 DIV.50 PRBS.5 PRBS.7 PRBS.9 PRBS.11 PRBS.13 PRBS.15 PRBS.21 PRBS.23 PRBS.31		
Pattern Choice per Transmit Channel	Per-transmitter		
Pattern Choice per Receive Channel	Per-receiver		
BERT Comparison Mode	Automatic seed generation for PRBS		Automatically aligns to PRBS data patterns.
User Programmable Pattern Memory			
Total Available Memory	2	GByte	Memory allocation is customizable. Contact factory.
Individual Force Pattern	Per-transmitter		
Individual Expected Pattern	Per-receiver		
Minimum Pattern Segment Size	512	bits	
Maximum Pattern Segment Size	65536	bits	
Total Memory Space for Transmitters	1	Mbits	Memory allocation is customizable. Contact factory.
Total Expected Memory Space for Receivers	1	Mbits	Memory allocation is customizable. Contact factory.
Pattern Sequencing			
Sequence Control	Loop infinite Loop on count Play to end		
Number of Sequencer Slots per Pattern Generator	4		This refers to the number of sequencer slots that can operate at any given time. The instrument has storage space for 16 different sequencer programs.
Maximum Loop Count per Sequencer Slot	$2^{16} - 1$		
Additional Pattern Characteristics			
Pattern Switching	Wait to end of segment Immediate		When sourcing PRBS patterns, this option does not exist.
Raw Data Capture Length	8192	bits	

Table 9 Measurement and Throughput Characteristics

Parameter	Value	Units	Description and Conditions
BERT Sync			
Alignment Modes	Pattern PRBS		Module can align to any user pattern or preset pattern.
Minimum SYNC Error Threshold	3	bits	
Maximum SYNC Error Threshold	2^{32}-1	bits	
Minimum SYNC Sample Count	1024	bits	
Maximum SYNC Sample Count	2^{32}	bits	
SYNC Time	20	ms	Assumes a PRBS7 pattern that is stored in a user pattern segment and worst case misalignment between DUT pattern and expected pattern; data rate is 3.25 Gbps.
BERT			
Error Counter Size	32	bits	Sample counts in the BERT are programmed in increments of 32 bits.
Maximum Single-Shot Duration	2^{32}-1	bits	Repeat mode is available to continuously count over longer durations.
Continuous Duration	Indefinite		
Alignment			
CDR Lock Time	5	us	
Self-Alignment Time	50	ms	

Table 10 Instruction Sequence Cache

Parameter	Value	Units	Description and Conditions
Simple Instruction Cache			
Instruction Learn mode Instruction	Start Stop Replay		
Advanced Instruction Cache			
Local Instruction Storage	1M Instructions		
Instruction Sequence Segments	1000		

Table 11 DUT Control Capabilities

Parameter	Value	Units	Description and Conditions
DUT IEEE-1149-1 (JTAG) Port (Option)			
JTAG-Port Transmit Signals	TCK		
	TRST		
	TDI		
JTAG-Port Receive Signals	TDO		
JTAG-Port Transmit Voltage Swing (Fixed)	0 to 2.5	V	
JTAG-Port Receive Max Voltage Swing	0 to 2.5	V	
TDI Bit Memory	4k		
TDO Bit Memory	4k		
DUT SPI Port (Option)			
SPI Signals	SCLK		
	SSN		
	MISO		
	MOSI		
Voltage Swing (Fixed)	0 to 2.5	V	

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1.0	Document release	Feb 27, 2013
1.1	Updated jitter injection specs, SSC specs, clock recovery specs; added block diagram descriptions	Oct 07, 2013
1.2	Minor edits	Oct 07, 2013
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