PCI Express Test

PCI Express Evolution and Challenges

PCIe Version	1.0a	1.1	2.0	3.0
Data Rate	2.5 Gbps per lane	2.5Gbps per lane	5.0 Gbps per lane	8.0 Gbps per lane
Data Encoding	8b/10b	8b/10b	8b/10b	Scrambling
Challenges	Transmitter test	Transmitter test	Receiver test	Receiver test, scrambling

Broadly adopted standard for high performance data links

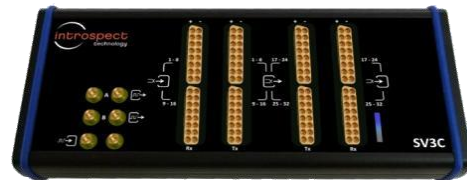Finding adoption in embedded applications and diverse environments

Physical layer test requirements are largely unchanged

Larger need for system-level protocol exerciser tests
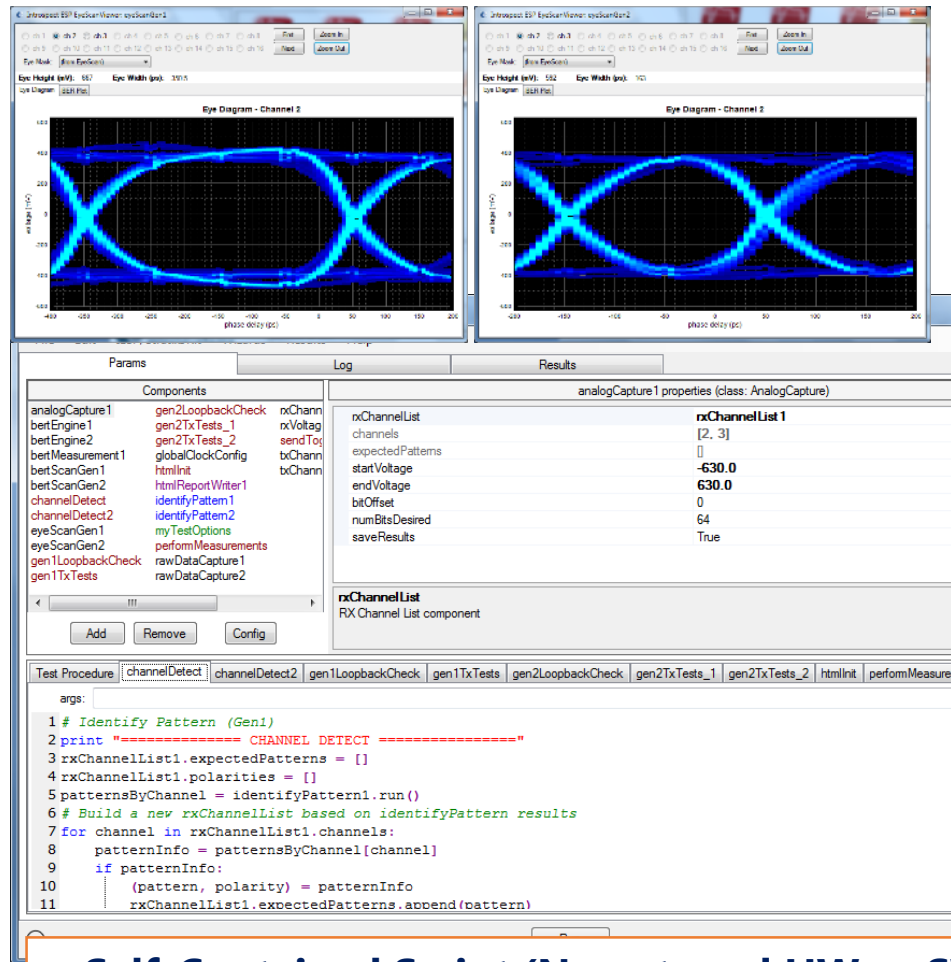
Introspect Solutions for PCI Express

| SV1C	SV3C	SV1D	SV3D
Benchtop tool / connects with DUT through cables	Benchtop tool / connects with DUT through cables	Tester on board / tester on backplane (no cables)	Tester on board / tester on backplane (no cables)
8 Lanes (Tx/Rx) + Clock	32 Lanes (Tx/Rx) + Clock	8 Lanes (Tx/Rx)	32 Lanes (Tx/Rx)
• Component phy-level validation • Component phy-level validation on CBB* • Add-in card phy-level validation on CBB* • System-level (protocol) exerciser test	• Component phy-level validation • Component phy-level validation on CBB* • Add-in card phy-level validation on CBB* • System-level (protocol) exerciser test	• Component phy-level production test on ATE • Board-level test on backplane • System-level (protocol) exerciser test	• Component phy-level production test on ATE • Board-level test on backplane • System-level (protocol) exerciser test

*CBB: Compliance Base Board (sold by PCI-SIG). Standard test board with cable connectors.

Bench-Top Setup (with CBB)

SV1C Tester (driving PCIe Ref Clock on CBB)
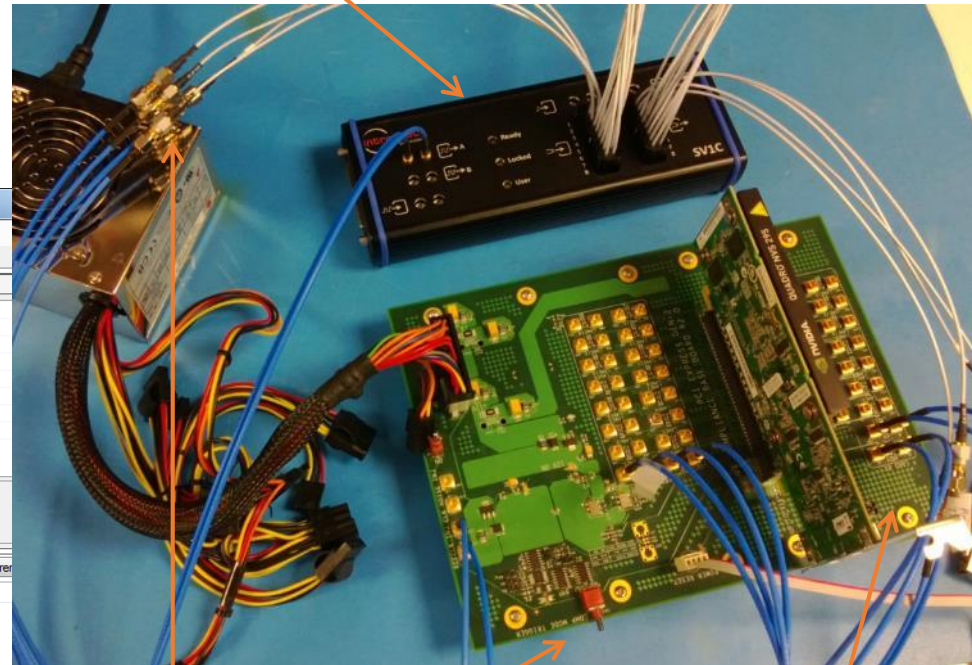
CBB

PCIe Test of x2 Lane Tx and Rx

Self-Contained Script (No external HW or SW)

Bench-Top Setup (with CBB)

Self-contained tester allows for both Tx and Rx verification

Receiver jitter tolerance test

Transmitter eye opening test
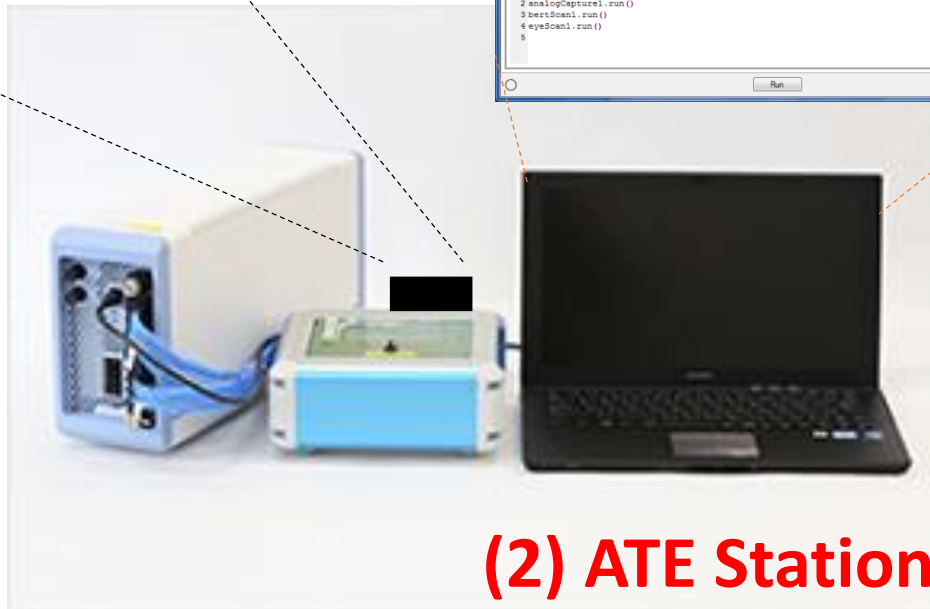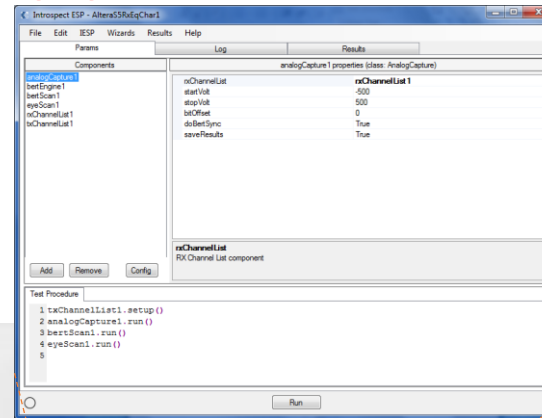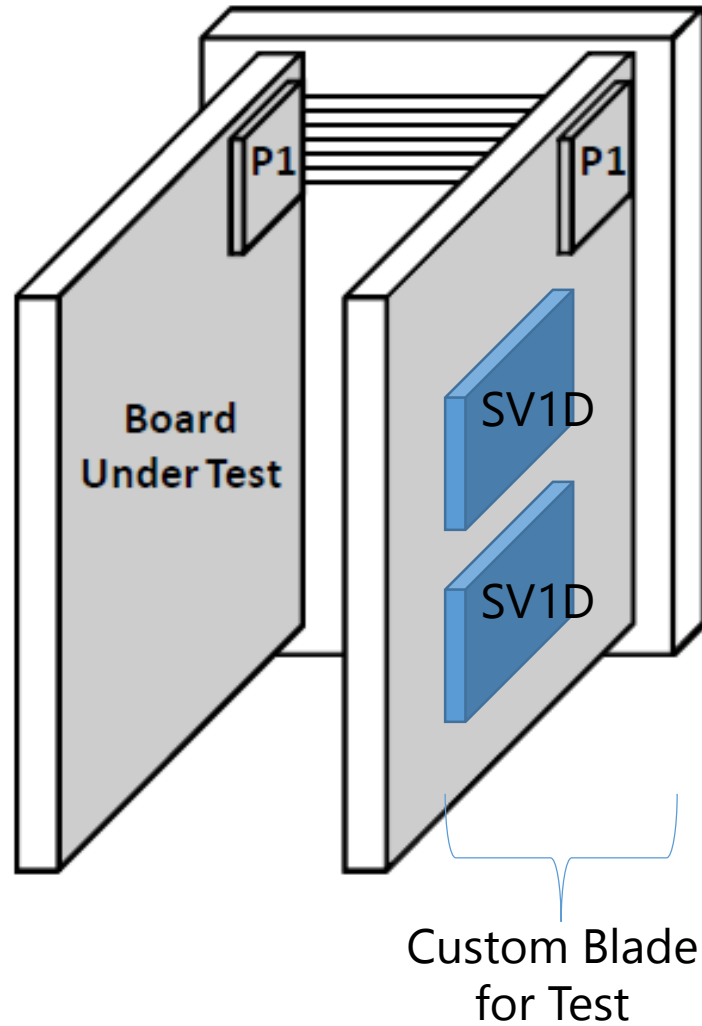
System-level (exerciser) protocol test

ATE Setup

(1) SV1D on Board

(5) IESP GUI

Self-contained tester allows for both Tx and Rx verification

Receiver jitter tolerance test

Transmitter eye opening test

System-level (exerciser) protocol test

(2) ATE Station

Embedded/Backplane with Cable Instrument Setup

Custom enclosure designed by customer

Backplane under test

Embedded/Backplane with Tester on Board Setup

- SV1D/SV3D: "Test Card"
  - 8/32 lane, 14 Gbps – Mezzanine Module
  - Removable and Reusable
  - **Application PCB or ATE PCB**

Bottom View (smaller than iphone 5S)

System-Level Exerciser Test
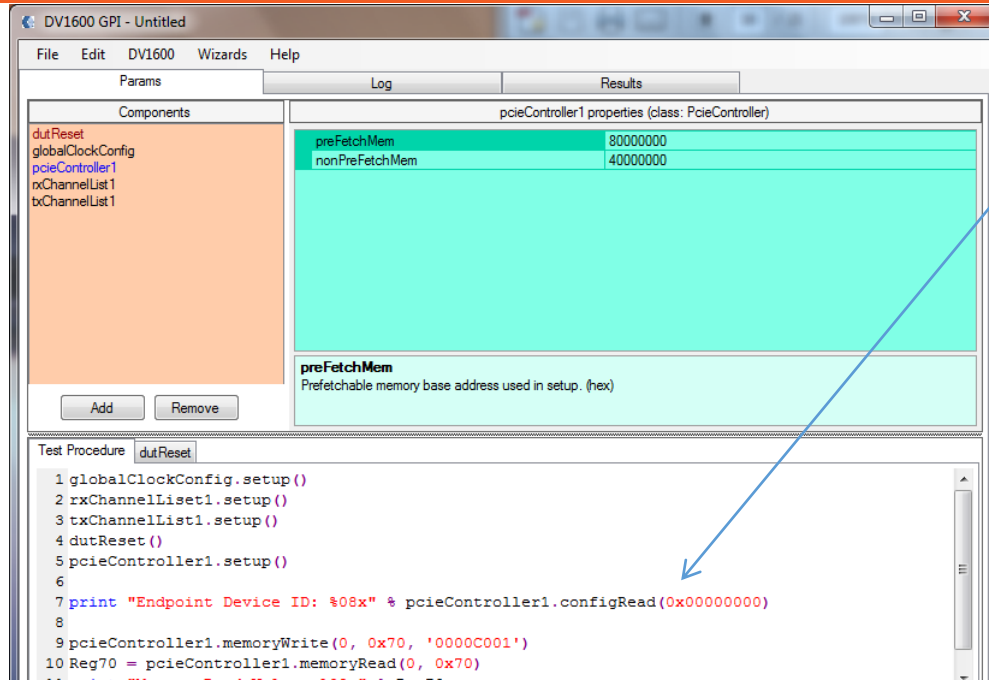
Script-based Read/write testing and result logging

Summary

Introspect offers SerDes transmitter and receiver test solutions that are well-suited for PCI Express validation and production

Tools allow for ultra-compact and low cost setups

Introspect product form factor options allows for deployment in embedded applications such as VPX, ATCA

Thank You!

www.introspect.ca